ATARI 810 DISK
PERIPHERAL DEVICE DESCRIPTION

Preliminary release (9-DEC-80)
Revision A (15-DEC-80)

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1. Functional description of 810

Section 1 provides a functional description of Revision B of the Atari Model 810 Disk peripheral.

1.1 General description

There are several obscure terminologies used in this manual, as explained in the paragraphs that follow.

Hexadecimal numbers -- Any number in this document is to be read as decimal unless: 1) the number is preceded by a dollar sign ('$'), or 2) the number is a memory or I/O port address. In both of those cases the number is to be read as hexadecimal. For example $43 is a hexadecimal number and 07FF will be a hexadecimal address within context.

Negative logic -- A few of the serial bus signals are true when low instead of when high; a signal of this type is identified by following its name with a minus sign ('-'). For example, read COMMAND- as COMMAND BAR or COMMAND NOT.

1.2 Overall system performance

1.2.1 Capacity of media

The Model 810 is designed to accommodate a single single-sided 5 1/4 inch mini-floppy diskette with soft sectoring. Each diskette is formatted to contain 40 tracks of 18 sectors each, with each sector containing 128 data bytes plus overhead; the data capacity of a diskette is thus 92,160 bytes.

1.2.2 Organization and format of data on media

As stated in the preceding paragraph, the disk is formatted to contain 40 tracks, each track containing 18 sectors plus an index field. The outermost track is called track 0 and the innermost track is called track 39, with the track centers being separated by 1/48 inch.

The sectors on each track are numbered from 1 to 18 and are physically ordered (initially formatted) with an interleave factor of 7, as shown below, with the index field immediately preceding sector number 18:

18,7,14,3,10,17,6,13,2,9,16,5,12,1,8,15,4,11

Each sector is comprised of a pre-sector gap, an ID field, a data field and a post-sector gap; with the post-sector gap of one sector being contiguous with the pre-sector gap of the next (with the exception of the sector 11/18 gap, which is undefined). The ID and the data fields are in the standard IBM 3740 format, the gaps are not; the formats for these items are described in the paragraphs that follow.

Index field

The index field is comprised of:

256 bytes of zeroes.
1 byte of Index Address Mark.
11 bytes of zeroes.

The Index Address Mark is generated by the FD1771 Floppy Disk Controller in response to a command from the controller to do so. This Address Mark is a single byte in length.

Pre-sector gap

The pre-sector gap is comprised of:

6 bytes of zeroes.

ID field

The sector ID field is comprised of:

1 byte of ID Address Mark.
1 byte of track number ($00-27).
1 byte of zeroes.
1 byte of sector number ($01-12).
1 byte of zeroes (indicates the sector size = 128).
2 bytes of CRC (G(x) = x**16 + x**12 + x**5 + 1).

The ID Address Mark is generated by the FD1771 in response to a command from the controller to do so. This Address Mark is a single byte in length.

The ID field CRC is generated by the FD1771 and includes all information starting with the ID Address Mark and up to the 2 CRC bytes.

Data field

The sector data field is comprised of:

17 bytes of zeroes (pre-data field gap).
1 byte of Data Address Mark.
128 bytes of data.
2 bytes of CRC (G(x) = x**16 + x**12 + x**5 + 1).

The Data Address Mark is generated by the FD1771 is response to a command from the controller to do so. This Address Mark is a single byte in length.

The data field CRC is generated by the FD1771 and includes all information starting with the Index Address Mark and up to the 2 CRC bytes.

Post-sector gap

The post-sector gap is comprised of:

9 bytes of all zeroes.
3 bytes of all ones.

The recording technique used to physically store bits on the

media is Frequency Modulation (FM) with a clock pulse being generated for each data bit (except in the case of the special Address Marks); the combined clock pulse and data pulse is referred to as a "cell". The pulses are recorded at a rate of 250,000 pulses per second (1 MHz clock divided by 4) yielding a cell read/write data rate of 125,000 bits per second. Since the data is recorded at fixed frequencies, and since the linear track size decreases as the head is moved toward the center of the disk, the recording density increases on the inner tracks.

1.2.3 Data throughput rates

Throughput is determined from disk latency, disk data transfer time and serial bus transfer time (plus sector data verification for some operations).

Rotational latency

The worst case rotational latency is the time for the disk to make one full rotation; this time is 60 sec/min / 305 rpm = 197 milliseconds. The average case latency is half that figure, or 98 milliseconds.

Sector data transfer time

The time to transfer a sector of information to or from the FD1771, from or to the disk controller, is on the order of 10 milliseconds.

Serial bus transfer time

The time to transfer a complete serial bus command sequence on the serial bus is on the order of 70 milliseconds.

Data throughput rates

The best case throughput of a single sector will be 80 milliseconds.

The average case throughput of a single sector will be 180 milliseconds.

The worst case throughput of a single sector will be 280 milliseconds (assuming no errors).

The presence of errors in either the serial bus communication or disk I/O will, of course, add additional time to any operation.

1.2.4 Operating modes and options

The Model 810 is to be operational as soon as it is powered on; the controller passively monitors the serial I/O bus looking for a command from the PCS directed to the specific unit set by the switches at the back of the 810. When a period of approximately 7 seconds has elapsed since the completion of the last command to a given unit, the controller firmware will step the head to

track 39 and turn off the drive motor. When a new command is received for a unit which has the drive motor turned off, the drive motor will be turned on again.

Unit number selection

There are two switches at the back of the unit which provide a logical unit (1-4) selection mechanism; this feature allows up to four 810s to be resident on the serial bus and to be uniquely identified. The logical unit selection is completely independent of the physical unit ordering on the serial bus.

Diskette write protection

There is a sensor in each unit which senses the opacity of a section of the diskette cover. When the section is opaque the disk is not to be written to or formatted; when the section is transparent the disk may be written to or formatted. A disk may always be read.

1.2.5 Expandability

There are no special provisions for expansion provided.

1.3 Serial bus interface specifications

This section describes the 810 device specific portions of the serial bus interface; see Appendix A for the general serial bus protocol.

The media is organized by track and sector as explained in section 1.2.2, but the serial bus commands utilize a sector address called the logical sector number, where the sector numbers range from 1 to 720. The sector numbers map to track/sector addresses using the integer equations:

```
track =  ( logical sector number - 1 ) / 18.
sector = ( ( logical sector number - 1 ) MOD 18 ) + 1.
```

There are five commands supported by the disk controller:

```
GET SECTOR
PUT SECTOR
PUT SECTOR WITH VERIFY
STATUS REQUEST
FORMAT DISK
```

1.3.1 GET SECTOR

The controller receives a command frame containing the following information:

```
Device I.D. = $31-34.
Command byte = $52.
```

Auxilliary 1 = sector number (lsb).
Auxilliary 2 = sector number (msb).
Command frame checksum.

The controller then attempts to read the indicated sector and, if successful, returns a COMPLETE byte followed by a data frame consisting of the 128 sector data bytes followed by the frame checksum.

1.3.2 PUT SECTOR

The controller receives a command frame containing the following information:

Device I.D. = $31-34.
Command byte = $50.
Auxilliary 1 = sector number (lsb).
Auxilliary 2 = sector number (msb).
Command frame checksum.

The controller then acknowledges the command frame and waits for a data frame. When the data frame is received, it is first acknowledged and then the frame data is written to the specified sector and finally a COMPLETE byte is sent.

1.3.3 PUT SECTOR WITH VERIFY

The controller receives a command frame containing the following information:

Device I.D. = $31-34.
Command byte = $57.
Auxilliary 1 = sector number (lsb).
Auxilliary 2 = sector number (msb).
Command frame checksum.

The controller then acknowledges the command frame and waits for a data frame. When the data frame is received, it is first acknowledged and then the frame data is written to the specified sector, the sector is then verified, and finally a COMPLETE byte is sent.

1.3.4 GET STATUS

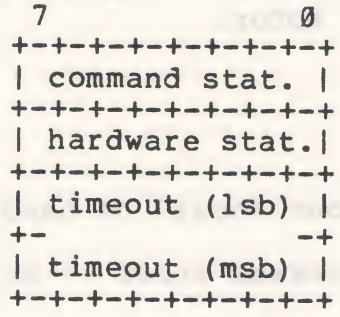
The controller receives a command frame containing the following information:

Device I.D. = $31-34.
Command byte = $53.
Auxilliary 1 = N/A.
Auxilliary 2 = N/A.
Command frame checksum.

The controller formats a four byte status frame and sends it to

the serial bus preceded by a COMPLETE byte and followed by a checksum of the frame.

The status frame format is shown below:



The command status contains the following status bits:

Bit-Ø = 1 indicates an invalid command frame was received.
Bit-1 = 1 indicates an invalid data frame was received.
Bit-2 = 1 indicates that an operation was unsuccessful.
Bit-3 = 1 indicates that the disk is write protected.
Bit-4 = 1 indicates active/standby (motor on/off).

The hardware status byte contains the inverted value of the status register of the FD1771 Floppy Disk Controller, for the last command issued. See Appendix B for information relating to the meaning of each bit in the byte.

The timeout byte contains a controller provided maximum timeout value (in seconds), for the worst case command, to be used by the handler. The worst case operation is a disk format, and the timeout value is $ØØEØ (224 seconds).

1.3.5 FORMAT DISK

The controller receives a command frame containing the following information:

Device I.D. = $31-34.
Command byte = $21.
Auxilliary 1 = N/A.
Auxilliary 2 = N/A.
Command frame checksum.

The controller acknowledges the command frame and then attempts to format the entire disk and to verify it. All bad logical sector numbers, up to a maximum of 63 numbers, are returned in a standard 128 byte data frame; two bytes of all ones ($FFFF) follow the last bad sector number returned.

1.4 Operating modes and transient behaviors

1.4.1 Power-up

In response to a power-up of the Model 810, the controller

firmware will do the following:

Turn on the drive motor.
Position the head to track 0.
Wait for a command, or after 7 seconds step in to track 39 and turn off the drive motor.

1.4.2 Error handling

The following error conditions should be handled as indicated.

Serial bus command frame checksum error -- No response.

Serial bus command frame sector number out of range -- Send NAK.

Serial bus data frame checksum error -- Send NAK.

Write command to protected diskette -- Send ACK after command frame and ERR after data frame.

Read error while reading a sector -- Try to read up to 4 times; if no success send ERR.

Write error while writing a sector -- Try to write up to 4 times; if no success send ERR.

Read after write verify error -- Send ERR.

Format write error (timeout) -- Send ERR and then send a data frame with the first two bytes equal to all ones.

Format verify error -- Save the logical sector number in an internal buffer, and when the verify operation is complete or the buffer fills, send ERR and then send the bad sector addresses as described in section 1.3.5.

Inability to find indicated sector (timeout) -- If the sector is not found within 500 milliseconds after positioning to the correct track, the operation is retried. If that retry fails, seek to the reference track (track 0), then seek to the desired track and try up to 4 more times. If the sector still cannot be found, send ERR.

1.4.3 Soft RESET

There is no hardware facility for generating a soft RESET; the unit may be RESET by cycling the Model 810 power ON/OFF switch.

1.5 Diagnostic requirements

There are no requirements for built-in diagnostics for the Model 810.

1.6 Configurations/options supported

There is a single configuration/option parameter for the Model 810 and that is the logical unit number select. There are a pair of switches at the back of the unit which are used to indicate which of the four possible logical units (1-4) this unit is to become. These switches are to be checked as part of the processing of each command frame.

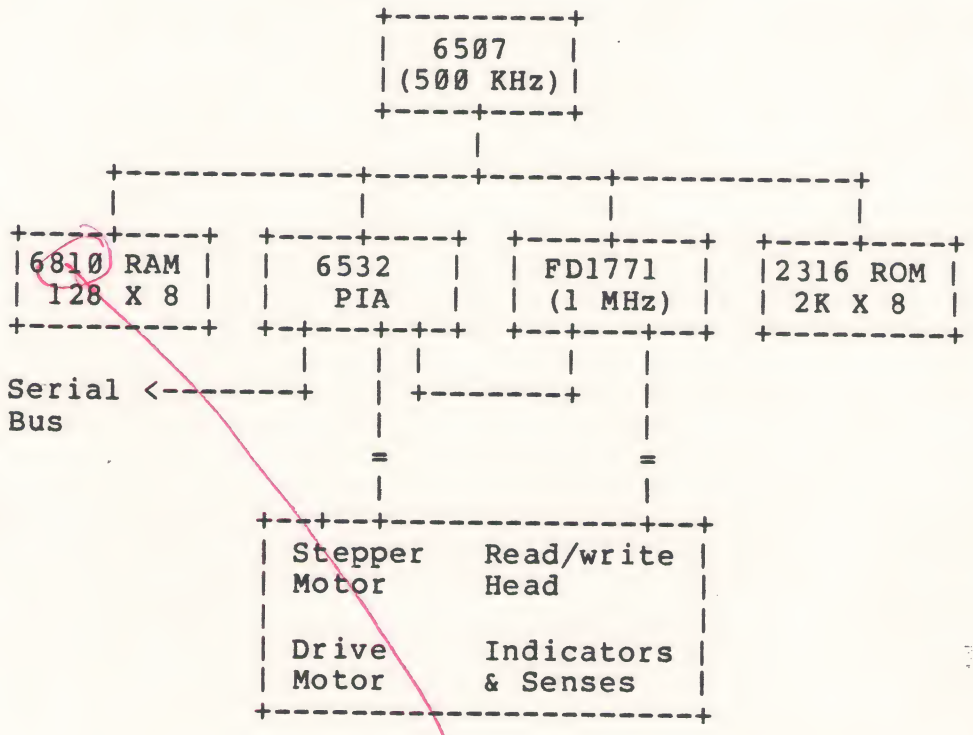
2. Hardware description

2.1 General description

The Model 810 is comprised of a Micro Peripherals Inc. mini-floppy diskette drive and an Atari designed and built controller board mounted together in a single package.

2.2 Block diagram

A block diagram of the controller is shown below:



2.3 Controller memory and I/O address assignments

```
ROM address space = 0800-0FFF (2316).
RAM address space = 0080-00FF (6810)
                    0180-01FF (6532).
I/O address space = 0000-0003 (FD1771)
                    0380-039F (6532).
```

2.4 I/O interface specification

2.4.1 Parallel I/O ports

All of the I/O for the controller processor is performed via two sets of memory mapped I/O ports; one set is assigned to a FD1771 Floppy Disk Controller chip and the other set is assigned to a 6532 PIA chip. The ports are described further in the sections that follow.

2.4.1.1 FD1771 Floppy Disk Controller chip

The FD1771 chip data access lines expect and provide data in bit complemented form (1 for 0 and 0 for 1); since there is no hardware inversion of the data bus between the 6507 and the FD1771, the inversion must be performed by the controller firmware. The descriptions in this section, as well as those to be found in Appendix B, describe the data as seen inside the FD1771, which is the complement of the data as seen by the 6507.

The memory mapped port address assignments are shown below:

Address	Direction	Function
0000	READ	Status register.
0000	WRITE	Command register.
0001	RD/WRT	Track register.
0002	RD/WRT	Sector register.
0003	READ	Read data register.
0003	WRITE	Write data register.

The description of the FD1771 chip is to be found in Appendix B.

2.4.1.2 6532 Peripheral Interface Adaptor (PIA)

The memory mapped port address assignments are shown below:

Address	Direction	Function
0380	RD/WRT	Port A.
0381	WRITE	Port A data direction register.
0382	RD/WRT	Port B.
0383	WRITE	Port B data direction register.
0384	(WRITE)	Negative edge detect, disable int.
0385	(WRITE)	Positive edge detect, disable int.
0385	READ	Read and clear interrupt flag.
0386	(WRITE)	Negative edge detect, enable int.
0387	(WRITE)	Positive edge detect, enable int.
039X	(WRITE)	Interval timer setup.

The bit assignments to the 6532 are shown below, by port:

Port	Bit-#	Direction	Function
0380	7	READ	1 = data request from FD1771.
	6	READ	1 = FD1771 IRQ.
	5	N/A	unused.
	4	READ	1 = diskette write protected.
	3	N/A	unused.
	2	READ	Drive select switch #2 (Note 1).
	1	WRITE	1 = drive motor on/drive select.
	0	READ	Drive select switch #1 (Note 1).
0381	7-0	WRITE	Port 0380 data direction select: 1 = PIA output pin, 0 = PIA input pin.

Note 1 -- The drive select switch values are mapped to logical unit numbers as shown in the table below:

Switch #2	Switch #1	Logical unit
1	1	1
1	Ø	2
Ø	Ø	3
Ø	1	4

Port	Bit-#	Direction	Function
Ø382	7	READ	Serial bus data input (inverted).
	6	READ	Serial bus NOT COMMAND- (1=command).
	5	WRITE	Stepper motor phase 4 (Note 2).
	4	WRITE	Stepper motor phase 3 (Note 2).
	3	WRITE	Stepper motor phase 2 (Note 2).
	2	WRITE	Stepper motor phase 1 (Note 2).
	1	READ	Serial bus +5V/READY (Ø=READY).
	Ø	WRITE	Serial bus data output (data true). (Note 3).
Ø383	7-Ø	WRITE	Port Ø382 data direction select: 1 = PIA output pin, Ø = PIA input pin.

Note 2 -- See section 2.5.1 for a description of the stepper motor characteristics.

Note 3 -- The serial bus data output line is to be switched from a PIA output line to an input line whenever the controller is not outputting data to the serial bus.

The ports below all relate to internal functions of the 6532 PIA; the ports designated '(WRITE)' do not operate upon the write data, the command is entirely encoded in the address (as explained in Appendix C).

Port	Bit-#	Direction	Function
Ø384		(WRITE)	Negative edge detect, disable int.
Ø385		(WRITE)	Positive edge detect, disable int.
Ø385		READ	Read and clear interrupt flag.
Ø386		(WRITE)	Negative edge detect, enable int.
Ø387		(WRITE)	Positive edge detect, enable int.
Ø39X		(WRITE)	Interval timer setup.

The description of the 6532 chip is to be found in Appendix C.

2.4.2 Serial I/O ports

There are no general purpose serial I/O ports provided in the Model 810.

2.4.3 Interruts

There is no interrupt capability in the 6507 processor chip.

2.5 Electromechanical components

2.5.1 Head stepper motor

The continuous stepper motor sequence for head inward movement is shown below; the sequence in reverse order provides head outward movement:

Phase4	Phase3	Phase2	Phase1	Track # mod 4
1	1	Ø	Ø	Ø
Ø	1	1	Ø	1
Ø	Ø	1	1	2
1	Ø	Ø	1	3
1	1	Ø	Ø	Ø
etc.				

When the stepper has been positioned to track Ø, the phase values must be 1 1 Ø Ø.

When the stepper is not being used the phases should all be set to zero; no phase value combinations other than zero and the values shown in the table should be used.

The minimum delay between steps for reliable operation is 5.25 milliseconds. + settle time

The reference track is track Ø, which may be reached by stepping outward a calculated number of tracks from a known track or by stepping outward some arbitrarily large number that guarantees that track zero is reached. No harm is done by driving the stepper beyond track Ø (attempting to position the head beyond track Ø) as there is a stop which will restrain the head, without causing any damage to the head or to the stepper.

The inter-track spacing is 1/48 inch, which is equivalent to 1 step.

2.5.2 Diskette drive motor

The operational speed for the drive motor is 305 RPM.

The time required for the motor to get to operational speed from a dead stop is 200 milliseconds.

3. Firmware description

3.1 General description

3.2 Command descriptions

3.3 Special considerations

3.4 Data base description

3.5 Module hierarchy

3.6 Procedure descriptions

Appendix A -- Serial I/O Bus Characteristics and Protocol

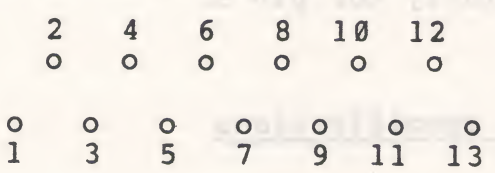
This appendix describes the electrical characteristics of the Atari 400/800 serial bus, the use of the bus to send bytes of data, the organization of the bytes as "frames" (records), and the overall command sequences which utilize frames and response bytes to provide computer/peripheral communication. All signal direction terminology assumes the viewpoint of the PCS computer (e.g. in/out, receive/send, etc.).

Hardware/electrical characteristics

The Atari 400/800 computer communicates with peripheral devices over a 19,200 baud asynchronous serial port. The serial port consists of a serial DATA OUT (transmission) line, a serial DATA IN (receiver) line and other miscellaneous control lines.

Data is transmitted and received as 8 bits of serial data (LSB sent first) preceded by a logic zero start bit and succeeded by a logic one stop bit. The serial DATA OUT is transmitted as positive logic (+4v = one/true/high, 0v = zero/false/low). The serial DATA OUT line always assumes its new state when the serial CLOCK OUT line goes high; CLOCK OUT then goes low in the center of the DATA OUT bit time.

An end view of the serial bus connector at the computer or peripheral is shown below (the cable connectors would of course be a mirror image):



where: 1 = computer CLOCK IN.
2 = computer CLOCK OUT.
3 = computer DATA IN.
4 = GND.
5 = computer DATA OUT.
6 = GND.
7 = COMMAND-.
8 = MOTOR CONTROL.
9 = PROCEED-.
10 = +5v/READY.
11 = computer AUDIO IN.
12 = +12v.
13 = INTERRUPT-.

1 CLOCK IN is not used by the present O.S. and peripherals. This line can be used in future synchronous communications schemes.

2 CLOCK OUT is the serial bus clock. CLOCK OUT goes high at the start of each DATA OUT bit and returns to low in the middle of each bit.

3 DATA IN is the serial bus data line to the computer.

4 Pin 4 GND is the signal/shield ground line.

5 DATA OUT is the serial bus data line from the computer.

6 Pin 6 GND is the signal/shield ground line.

7 COMMAND- is normally high and goes low when a command frame is being sent from the computer.

8 MOTOR CONTROL is the cassette motor control line (high=on, low= off).

9 PROCEED- is not used by the present O.S. and peripherals (this line is pulled high passively inside the Model 800).

10 +5v/READY indicates that the computer is turned on and ready. This line may also be used as a +5 volt supply of 50 ma. current rating for Atari peripherals only.

11 AUDIO IN accepts an audio signal from the cassette.

12 Pin 12 is a +12 volt supply for Atari peripherals only.

13 INTERRUPT- is not used by the present O.S. and peripherals (this line is pulled high passively inside the Model 800).

There are no pin reassignments made in the serial bus cable, so pin 3, the computer's DATA IN line, is the peripheral's data output line; and similarly for pin 5.

Serial bus electrical specifications

Peripheral input:

VIH = 2.0v min.
VIL = 0.4v max.

IIH = 20ua. max. @ VIH = 2.0v
IIL = 5ua. max. @ VIL = .4v

Peripheral output (open collector bipolar):

V0L = 0.4v max. @ 1.6 ma.
V0H = 4.5v min. with external 100Kohm pull-up.

Vcc/READY input:

VIH = 2.0v min. @ IIH = 1ma. max.
VIL = 0.4v max.
Input goes to logic zero when open.

Bus commands

The bus protocol specifies that all commands must originate from the computer, and that peripherals will present data on the bus only when commanded to. Every bus operation will go to completion before another bus operation is initiated (no overlap). An error detected at any point in the command sequence will abort the entire sequence.

A bus operation consists of the following elements:

Command frame from the computer.

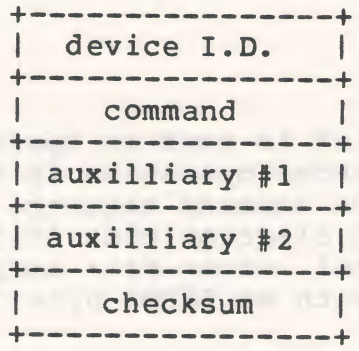
Acknowledgement (ACK) from the peripheral.

Optional data frame to or from the computer.

Operation complete (COMPLETE) from the peripheral.

COMMAND FRAME

The serial bus protocol provides for three types of commands: 1) data send, 2) data receive and 3) immediate (no data -- command only). There is a common element in all three types, a command frame consisting of five bytes of information sent from the computer while the COMMAND- line is held low. The format of the command frame is shown below:



The device I.D. specifies which of the serial bus devices is being addressed.

The command byte contains a device dependent command.

The auxilliary bytes contain more device dependent information.

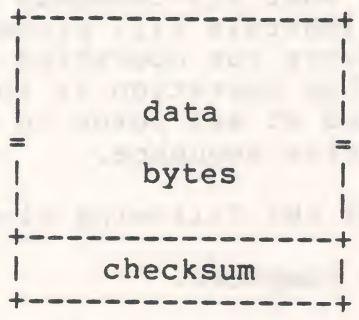
The checksum byte contains the arithmetic sum of the first four bytes (with the carry added back after every addition).

COMMAND FRAME ACKNOWLEDGE

The peripheral being addressed would normally respond to a command frame by sending an ACK byte ($41) to the computer. If there is a checksum error in the command frame, the peripheral should not respond; any other type of error should result in a NAK being sent.

DATA FRAME

Following the command frame (and ACK) may be an optional data frame which is formatted as shown below:



This data frame may originate at the computer or at the device controller, depending upon the command. Current device controllers expect fixed length data frames as does the computer, where the data frame length is a fixed function of the device type and command.

The checksum value in the data frame is the arithmetic sum of all of the frame data preceding the checksum, with the carry from each addition being added back (the same algorithm as for the command frame).

In the case of the computer sending a data frame to a peripheral, the peripheral is expected to send an ACK if the data frame is acceptable, and a NAK ($4E) if the data frame is unacceptable.

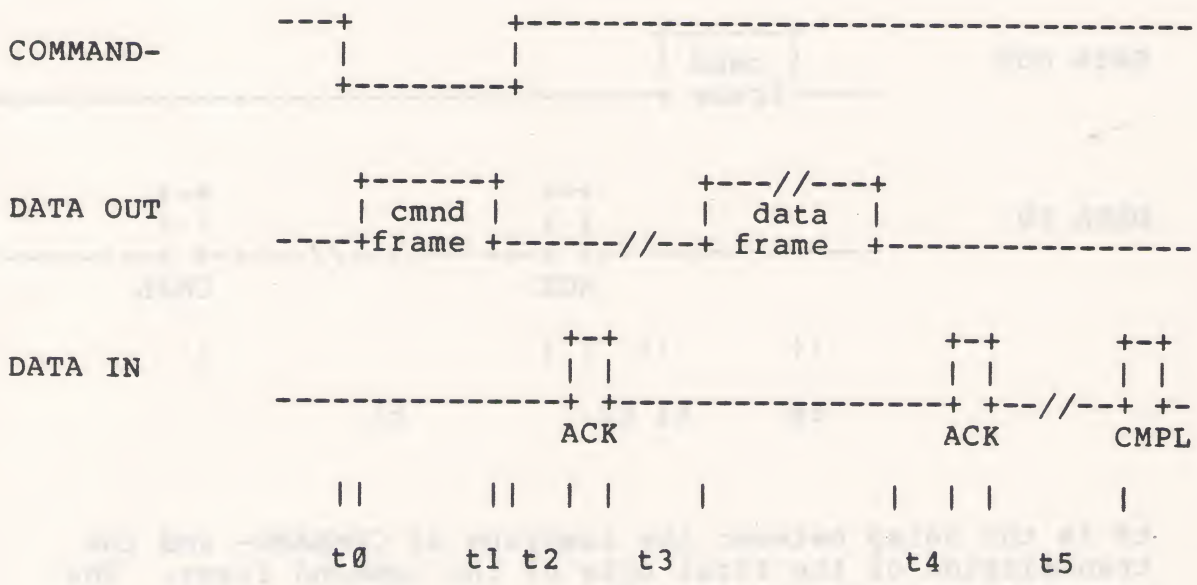
OPERATION COMPLETE

A peripheral is also expected to send an operation COMPLETE byte ($43) at the time the commanded operation is complete. The location of this byte in the command sequence for each command type is shown in the timing diagrams that follow. If the operation cannot go to normal, error-free completion, the peripheral should respond with an ERROR byte ($45) instead of COMPLETE.

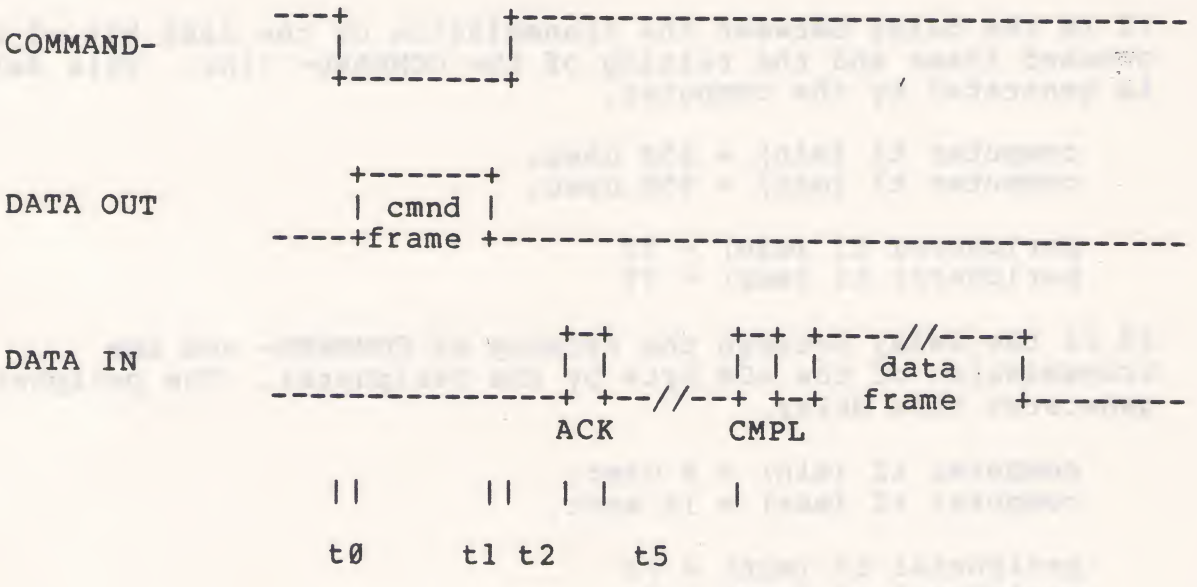
Bus timing

This section provides timing diagrams for the three types of command sequences: data send, data receive and immediate.

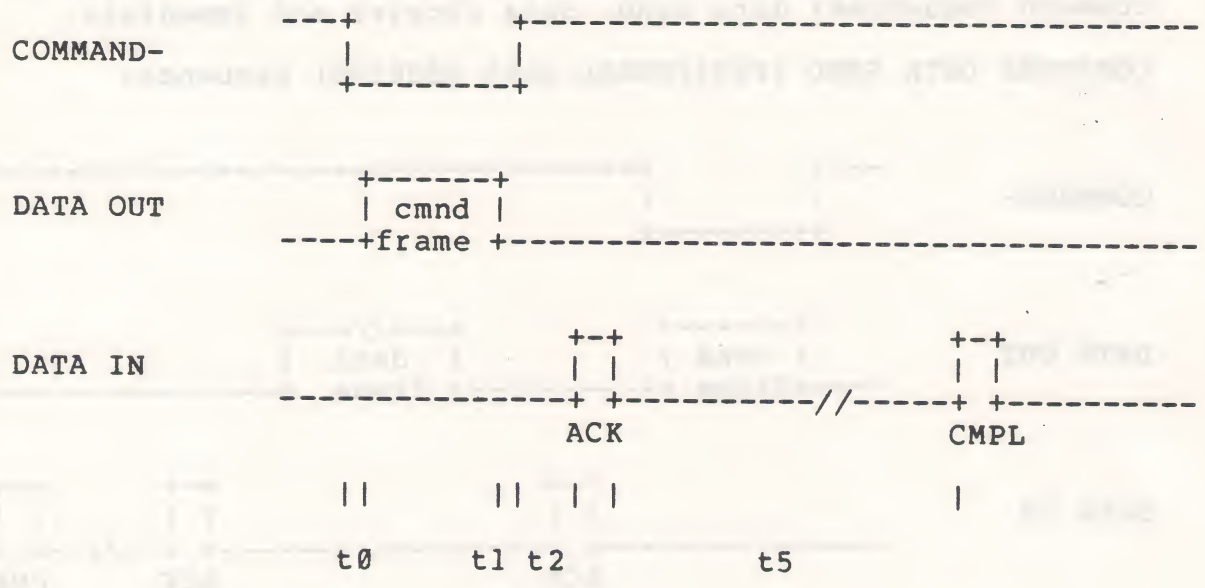
COMPUTER DATA SEND (PERIPHERAL DATA RECEIVE) sequence:



COMPUTER DATA RECEIVE (PERIPHERAL DATA SEND) sequence:



IMMEDIATE sequence:



t0 is the delay between the lowering of COMMAND- and the transmission of the first byte of the command frame. The computer generates this delay.

computer t0 (min) = 750 usec.
computer t0 (max) = 1600 usec.

peripheral t0 (min) = ??
peripheral t0 (max) = ??

t1 is the delay between the transmission of the last bit of the command frame and the raising of the COMMAND- line. This delay is generated by the computer.

computer t1 (min) = 650 usec.
computer t1 (max) = 950 usec.

peripheral t1 (min) = ??
peripheral t1 (max) = ??

t2 is the delay between the raising of COMMAND- and the transmission of the ACK byte by the peripheral. The peripheral generates this delay.

computer t2 (min) = 0 usec.
computer t2 (max) = 16 msec.

peripheral t2 (min) = ??
peripheral t2 (max) = ??

t3 is the delay between the receipt of the last bit of the ACK byte and the transmission of the first bit of the data frame by the computer. The computer generates this delay.

computer t3 (min) = 1000 usec.
computer t3 (max) = 1800 usec.

peripheral t3 (min) = ??
peripheral t3 (max) = ??

t4 is the delay between the transmission of the last bit of the data frame and the receipt of the first bit of the ACK byte by the computer. The peripheral generates this delay.

computer t4 (min) = 850 usec.
computer t4 (max) = 16 msec.

peripheral t4 (min) = ??
peripheral t4 (max) = ??

t5 is the delay between the receipt of the last bit of the ACK byte and the first bit of the COMPLETE byte by the computer. The peripheral generates this delay.

computer t5 (min) = 250 usec.
computer t5 (max) = 255 sec. (handler dependent)

peripheral t5 (min) = ??
peripheral t5 (max) = N/A

Serial bus special character values

ACK = $41.
NAK = $4E.
COMPLETE = $43.
ERR = $45.

Serial bus device I.D. to logical unit mapping (Model 810)

Unit 1 = $31.
Unit 2 = $32.
Unit 3 = $33.
Unit 4 = $34.

FD1771-01 Floppy Disk Formatter/Controller

FEATURES

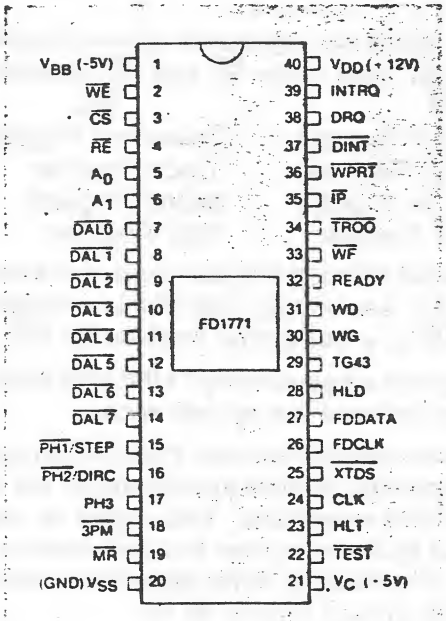
- SOFT SECTOR FORMAT COMPATIBILITY
- AUTOMATIC TRACK SEEK WITH VERIFICATION
- READ MODE
  Single/Multiple Sector Write with Automatic Sector Search or Entire Track Read
  Selectable 128 Byte or Variable Length Sector
- WRITE MODE
  Single/Multiple Sector Write with Automatic Sector Search
  Entire Track Write for Diskette Formatting
- PROGRAMMABLE CONTROLS
  Selectable Track-to-Track Stepping Time
  Selectable Head Settling and Head Engage Times
  Selectable Three Phase or Step and Direction and Head Positioning Motor Controls
- SYSTEM COMPATIBILITY
  Double Buffering of Data 8-Bit Bi-Directional Bus for Data, Control and Status
  DMA or Programmed Data Transfers
  All Inputs and Outputs are TTL Compatible

APPLICATIONS

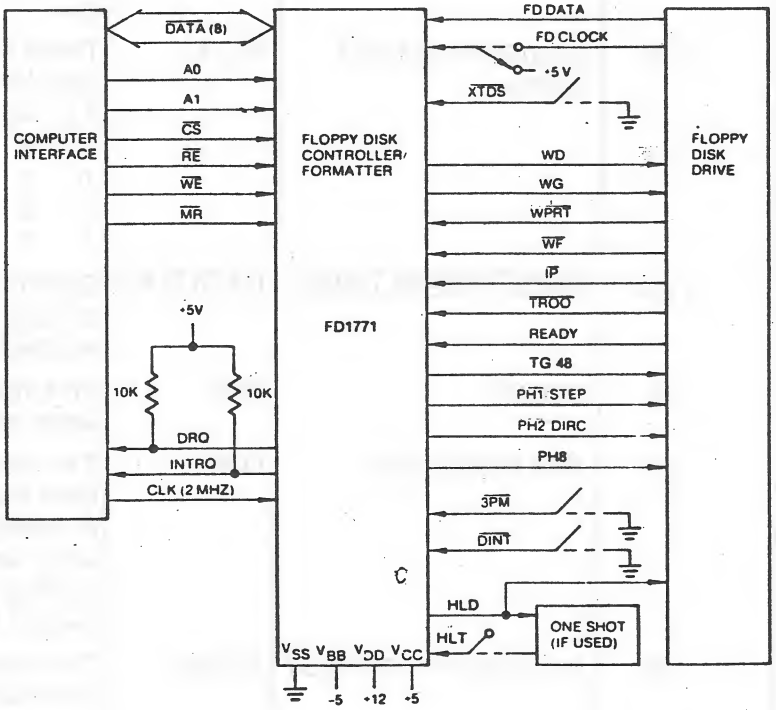
- FLOPPY DISK DRIVE INTERFACE
- SINGLE OR MULTIPLE DRIVE CONTROLLER/FORMATTER
- NEW MINI-FLOPPY CONTROLLER

GENERAL DESCRIPTION

The FD1771 is a MOS/LSI device that performs the functions of a Floppy Disk Controller/Formatter. The device is designed to be included in the disk drive electronics, and contains a flexible interface



PIN CONNECTIONS



FD1771 SYSTEM BLOCK DIAGRAM

organization that accommodates the interface signals from most drive manufacturers. The FD1771 is compatible with the IBM 3740 data entry system format.

The processor interface consists of an 8-bit bi-directional bus for data, status, and control word transfers. The FD1771 is set up to operate on a multiplexed bus with other bus-oriented devices.

The FD1771 is fabricated in N-channel Silicon Gate MOS technology and is TTL compatible on all inputs and outputs. The A and B suffixes are for ceramic and plastic packages, respectively.

PIN OUTS

Pin No.	Pin Name	Symbol	Function
1	Power Supplies	V_{BB}/NC	-5V
19	MASTER RESET	$\overline{MR}$	A logic low on this input resets the device and loads "03" into the command register. The Not Ready (Status bit 7) is reset during $\overline{MR}$ ACTIVE. When $\overline{MR}$ is brought to a logic high, a Restore Command is executed, regardless of the state of the Ready signal from the drive.
20		V_{SS}	Ground
21		V_{CC}	+5V
40		V_{DD}	+12V
Computer Interface			
2	$\overline{WRITE\ ENABLE}$	$\overline{WE}$	A logic low on this input gates data on the DAL into the selected register when $\overline{CS}$ is low.
3	$\overline{CHIP\ SELECT}$	$\overline{CS}$	A logic low on this input selects the chip and enables computer communication with the device.
4	$\overline{READ\ ENABLE}$	$\overline{RE}$	A logic low on this input controls the placement of data from a selected register on the DAL when $\overline{CS}$ is low.
5, 6	REGISTER SELECT LINES	A_0, A_1	These inputs select the register to receive/transfer data on the DAL lines under $\overline{RE}$ and $\overline{WE}$ control: A_1 A_0 $\overline{RE}$ $\overline{WE}$ 0 0 Status Register Command Register 0 1 Track Register Track Register 1 0 Sector Register Sector Register 1 1 Data Register Data Register
7-14	$\overline{DATA\ ACCESS\ LINES}$	$\overline{DAL0\text{-}DAL7}$	Eight bit inverted bidirectional bus used for transfer of data, control, and status. This bus is a receiver enabled by $\overline{WE}$ or a transmitter enabled by $\overline{RE}$.
24	CLOCK	CLK	This input requires a free-running 2 MHz ± 1% square wave clock for internal timing reference.
38	DATA REQUEST	DRQ	This open drain output indicates that the DR contains assembled data in Read operations, or the DR is empty in Write operations. This signal is reset when serviced by the computer through reading or loading the DR in Read or Write operation, respectively. Use 10K pull-up resistor to +5.
39	INTERRUPT REQUEST	INTRQ	This open drain output is set at the completion or termination of any operation and is reset when a new command is loaded into the command register. Use 10K pull-up resistor to +5.
Floppy Disk Interface:			
15	$\overline{Phase\ 1}$/Step	$\overline{PH1}$/STEP	If the $\overline{3PM}$ input is a logic low the three-phase motor control is selected and $\overline{PH1}$, $\overline{PH2}$, and PH3 outputs

Pin No.	Pin Name	Symbol	Function
16	$\overline{\text{Phase 2/Direction}}$	$\overline{\text{PH2}}$/DIRC	form a one active low signal out of three. $\overline{\text{PH1}}$ is active low after $\overline{\text{MR}}$. If the $\overline{\text{3PM}}$ input is a logic high the step and direction motor control is selected. The step output contains a 4 usec high signal for each step and the direction output is active high when stepping in; active low when stepping out.
17	Phase 3	PH3	
18	$\overline{\text{3-Phase Motor Select}}$	$\overline{\text{3PM}}$	
22	$\overline{\text{TEST}}$	$\overline{\text{TEST}}$	This input is used for testing purposes only and should be tied to +5V or left open by the user.
23	HEAD LOAD TIMING	HLT	The HLT input is sampled after 10 ms. When a logic high is sampled on the HLT input the head is assumed to be engaged.
25	$\overline{\text{EXTERNAL DATA SEPARATION}}$	$\overline{\text{XTDS}}$	A logic low on this input selects external data separation. A logic high or open selects the internal data separator.
26	FLOPPY DISK CLOCK (External Separation)	FDCLOCK	This input receives the externally separated clock when $\overline{\text{XTDS}}$ = 0. If $\overline{\text{XTDS}}$ = 1, this input should be tied to a logic high.
27	FLOPPY DISK DATA	FDDATA	This input receives the raw read disk data if $\overline{\text{XTDS}}$=1, or the externally separated data if $\overline{\text{XTDS}}$=0.
28	HEAD LOAD	HLD	The HLD output controls the loading of the Read-Write head against the media.
29	Track Greater than 43	TG43	This output informs the drive that the Read-Write head is positioned between tracks44-76. This output is valid only during Read and Write commands.
30	WRITE GATE	WG	This output is made valid when writing is to be performed on the diskette.
31	WRITE DATA	WD	This output contains both clock and data bits of 500 ns duration.
32	Ready	READY	This input indicates disk readiness and is sampled for a logic high before Read or Write commands are performed. If Ready is low, the Read or Write operation is not performed and an interrupt is generated. A Seek operation is performed regardless of the state of Ready. The Ready input appears in inverted format as Status Register bit 7.
33	$\overline{\text{WRITE FAULT}}$	$\overline{\text{WF}}$	This input detects wiring faults indications from the drive: When WG=1 and $\overline{\text{WF}}$ goes low, the current Write command is terminated and the Write Fault status bit is set. The $\overline{\text{WF}}$ input should be made inactive (high) when WG becomes inactive.
34	$\overline{\text{TRACK 00}}$	$\overline{\text{TR00}}$	This input informs the FD1771 that the Read-Write head is positioned over Track 00 when a logic low.
35	$\overline{\text{INDEX PULSE}}$	$\overline{\text{IP}}$	Input, when low for a minimum of 10 usec, informs the FD1771 when an index mark is encountered on the diskette.
36	$\overline{\text{WRITE PROTECT}}$	$\overline{\text{WPRT}}$	This input is sampled whenever a Write command is received. A logic low terminates the command and sets the Write Protect status bit.
37	$\overline{\text{DISK INITIALIZATION}}$	$\overline{\text{DINT}}$	The iput is sampled whenever a Write Track command is received. If $\overline{\text{DINT}}$=0, the operation is terminated and the Write Protect status bit is set.

ORGANIZATION

The Floppy Disk Formatter block diagram is illustrated on page 4. The primary sections include the parallel processor interface and the Floppy Disk interface.

Data Shift Register: This 8-bit register assembles serial data from the Read Data input (FDDATA) duriing Read operations and transfers serial data to the Write Data output during Write operations.

Data Register: This 8-bit register is used as a holding register during Disk Read and Write operations. In Disk Read operations the assembled data byte is transferred in parallel to the Data Register from the Data Shift Register. In Disk Write operations information is transferred in parallel from the Data Register to the Data Shift Register.

When executing the Seek command, the Data Register holds the address of the desired Track position. This register can be loaded from the DAL and gated onto the DAL under processor control.

Track Register: This 8-bit register holds the track number of the current Read/Write head position. It is incremented by one every time the head is stepped in (towards track 76) and decremented by one when the head is stepped out (towards track 00). The contents of the register are compared with the recorded track number in the ID field during disk Read, Write, and Verify operations. The Track Register can be loaded from or transferred to the DAL. This Register should not be loaded when this device is busy.

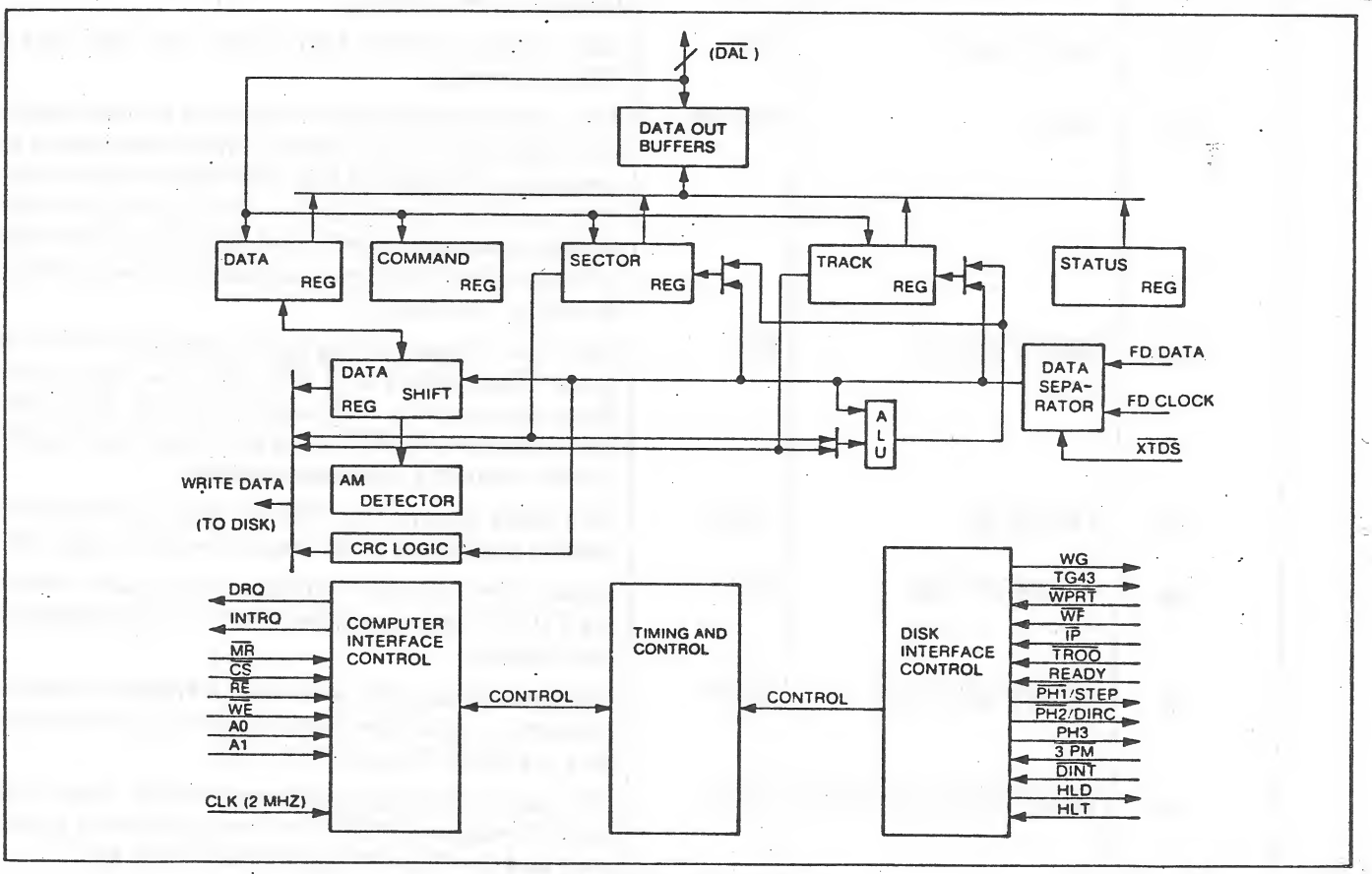
Sector Register (SR): This 8-bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk Read or Write operations. The Sector Register contents can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

Command Register (CR): This 8-bit register holds the command presently being executed. This register should not be loaded when the device is busy unless the execution of the current command is to be overridden. This latter action results in an interrupt. The command register can be loaded from the DAL, but not read onto the DAL.

Status Register (STR): This 8-bit register holds device Status information. The meaning of the Status bits are a function of the contents of the Command Register. This register can be read onto the DAL, but not loaded from the DAL.

CRC Logic: This logic is used to check or to generate the 16-bit Cyclic Redundancy Check (CRC). The polynomial is: $G(x) = x^{16} + x^{12} + x^5 + 1$.

The CRC includes all information starting with the address mark and up to the CRC characters. The CRC register is preset to ones prior to data being shifted through the circuit.



FD1771 BLOCK DIAGRAM

Arithmetic/Logic Unit (ALU): The ALU is a serial comparator, incrementer, and decrementer and is used for register modification and comparisons with the disk recorded ID field.

AM Detector: The Address Mark detector is used to detect ID, Data, and Index address marks during Read and Write operations.

Timing and Control: All computer and Floppy Disk Interface controls are generated through this logic. The internal device timing is generated from a 2.0 MHz external crystal clock.

PROCESSOR INTERFACE

The interface to the processor is accomplished through the eight Data Access Lines (DAL) and associated control signals. The DAL are used to transfer Data, Status, and Control words out of, or into the FD1771. The DAL are three-state buffers that are enabled as output drivers when Chip Select (CS) and Read Enable (RE) are active (low logic state) or act as input receivers when CS and Write Enable (WE) are active.

When transfer of data with the Floppy Disk Controller is required by the host processor, the device address is decoded and CS is made low. The least-significant address bits A1 and A0, combined with the signals RE during a Read operation or WE during a Write operation are interpreted as selecting the following registers:

A1-A0	READ ($\overline{RE}$)	WRITE ($\overline{WE}$)
0 0	Status Register	Command Register
0 1	Track Register	Track Register
1 0	Sector Register	Sector Register
1 1	Data Register	Data Register

During Direct Memory Access (DMA) types of data transfers between the Data Register of the FD1771 and the Processor, the Data Request (DRQ) output is used in Data Transfer control. This signal also appears as status bit 1 during Read and Write operations.

On Disk Read operations the Data Request is activated (set high) when an assembled serial input byte is transferred in parallel to the Data Register. This bit is cleared when the Data Register is read by the processor. If the Data Register is read after one or more characters are lost, by having new data transferred into the register prior to processor readout, the Lost Data bit is set in the Status Register. The Read operation continues until the end of sector is reached.

On Disk Write operations the Data Request is activated when the Data Register transfers its contents to the Data Shift Register, and requires a new data byte. It is reset when the Data Register is loaded with new data by the processor. If new data is not loaded at the time the next serial byte is required by the Floppy Disk, a byte of zeroes is written on the diskette and the Lost Data bit is set in the Status Register.

The Lost Data bit and certain other bits in the Status Register will activate the interrupt request (INTRQ). The interrupt line is also activated with normal completion or abnormal termination of all controller operations. The INTRQ signal remains active until reset by reading the Status Register to the processor or by the loading of the Command Register. In addition, the INTRQ is generated if a Force Interrupt command condition is met.

FLOPPY DISK INTERFACE

The Floppy Disk interface consists of head positioning controls, write gate controls, and data transfers. A 2.0 MHz ± 1% square wave clock is requred at the CLK input for internal control timing (may be 1.0 MHz for mini floppy).

HEAD POSITIONING

Four commands cause positioning of the Read-Write head (see Command Section). The period of each positioning step is specified by the r field in bits 1 and 0 of the command word. After the last directional step, an additional 10 milliseconds of head settling time takes place. The four programmable stepping rates are tabulated below.

The rates (shown in Table 1) can be applied to a Three-Phase Motor or a Step-Direction Motor through the device interface. When the $\overline{3PM}$ input is connected to ground, the device operates with a three-phase motor control interface, with one active low signal per phase on the three output signals $\overline{PH1}$, $\overline{PH2}$, and PH3. The stepping sequence, when stepping in, is Phases 1-2-3-1, and when stepping out, Phases 1-3-2-1. Phase 1 is active low after Master Reset. Note: PH3 needs an inverter if used.

The Step-Direction Motor Control interface is activated by leaving input $\overline{3PM}$ open or connecting it to +5V. The Phase 1 pin $\overline{PH1}$ becomes a Step pulse of 4 microseconds width. The Phase 2 pin $\overline{PH2}$ becomes a direction control with a high voltage on this pin indicating a Step In, and a low voltage indicating a Step Out. The Direction output is valid a minimum of 24 μs prior to the activation of the Step pulse.

When a Seek, Step or Restore command is executed, an optional verification of Read-Write head position can be performed by setting bit 2 in the command word to a logic 1. The verification operation begins at the end of the 10 millisecond settling time after the head is loaded against the media. The track number from the first encountered ID Field is compared against the contents of the Track Register. If the track numbers compare and the ID Field Cyclic Redundancy Check (CRC) is correct, the verify operation is complete. If track comparison is not

made but the CRC checks, an interrupt is generated, the Seek Error status (Bit 4) is set and the Busy status bit is reset.

Table 1. STEPPING RATES

r_1	r_0	1771-X1 CLK=2 MHz $\overline{TEST}$=1	1771-X1 CLK=1 MHz $\overline{TEST}$=1	1771 or -X1 CLK=2 MHz $\overline{TEST}$=0	1771 or -X1 CLK=1 MHz $\overline{TEST}$=0
0	0	6ms	12ms	Approx. 400us*	Approx. 800us*
0	1	6ms	12ms		
1	0	10ms	20ms		
1	1	20ms	40ms		

*For exact times consult WDC.

The Head Load (HLD) output controls the movement of the read/write head against the disk for data recording or retrieval. It is activated at the beginning of a Read, Write (E Flag On) or Verify operation, or a Seek or Step operation with the head load bit, h, a logic one remains activated until the third index pulse following the last operation which uses the read/write head. Reading or Writing does not occur until a minimum of 10 msec delay after the HLD signal is made active. If executing the type 2 commands with the E flag off, there is no 10 msec delay and the head is assumed to be engaged. The delay is determined by sampling of the Head Load Timing (HLT) input after 10 msec. A high state input, generated from the Head Load output transition and delayed externally, identifies engagement of the head against the disk. In the Seek and Step commands, the head is loaded at the start of the command execution when the h bit is a logic one. In a verify command the head is loaded after stepping to the destination track on the disk whenever the h bit is a logic zero.

DISK READ OPERATION

The 2.0 MHz external clock provided to the device is internally divided by 4 to form the 500 kHz clock rate for data transfer. When reading data from a diskette this divider is synchronized to transitions of the Read Data (FDDATA) input. When a transition does not occur on the 500 kHz clock active state, the clock divider circuit injects a clock to maintain a continuous 500 kHz data clock. The 500 kHz data clock is further divided by 2 internally to separate the clock and information bits. The divider is phased to the information by the detection of the address mark.

In the internal data read and separation mode the Read Data input toggles from one state to the opposite state for each logic one bit of clock or information. This signal can be derived from the amplified, differentiated, and sliced Read Head signal, or by the output of a flip-flop toggling on the Read Data pulses. This input is sampled by the 2 MHz clock to detect transitions.

The chip can also operate on externally separated data, as supplied by methods such as Phase Lock loop, One Shots, or variable frequency oscillators. This is accomplished by grounding the External Data Separator ($\overline{XTDS}$) INPUT. When the Read Data input makes a high-to-low transition, the information input to the FDDATA line is clocked into the Data Shift Register. The assembled 8-bit data from the Data Shift Register are then transferred to the Data Register.

The normal sector length for read or Write operations with the IBM 3740 format is 128 bytes. This format or binary multiples of 128 bytes will be adopted by setting a logic 1 in Bit 3 of the Read and Write commands. Additionally, a variable sector length feature is provided which allows an indicator recorded in the ID Field to control the length of the sector. Variable sector lengths can be read or written in Read or Write commands, respectively, by setting a logic 0 in Bit 3 of the command word. The sector length indicator specifies the number of 16 byte groups or 16 x N, where N is equal to 1 to 256 groups. An indicator of all zeroes is interpreted as 256 sixteen byte groups.

DISK WRITE OPERATION

After data is loaded from the processor into the Data Register, and is transferred to the Data Shift Register, data will be shifted serially through the Write Data (WD) output. Interlaced with each bit of data is a positive clock pulse of 0.5 μsec duration. This signal may be used to externally toggle a flip-flop to control the direction of Write Current flow.

When writing is to take place on the diskette the Write Gate (WG) output is activated, allowing current to flow into the Read/Write head. As a precaution to erroneous writing, the first data byte must be loaded into the Data Register in response to a Data Request from the FD1771 before the Write Gate signal can be activated.

Writing is inhibited when the $\overline{\text{Write Protect}}$ input is a logic low, in which case any Write command is immediately terminated, an interrupt is generated and the Write Protect status bit is set. The $\overline{\text{Write Fault}}$ input, when activated, signifies a writing fault condition detected in disk drive electronics such as failure to detect write current flow when the Write Gate is activated. On detection of this fault the FD1771 terminates the current command, and sets the Write Fault bit (bit 5) in the Status Word. The $\overline{\text{Write Fault}}$ input should be made inactive when the Write Gate output becomes inactive.

Whenever a Read or Write command is received the FD1771 samples the READY input. If this input is logic low the command is not executed and an interrupt is generated. The Seek or Step commands are performed regardless of the state of the READY input.

COMMAND DESCRIPTION

The FD1771 will accept and execute eleven commands. Command words should only be loaded in the Command Register when the Busy status bit is off (status bit 0). The one exception is the Force Interrupt command. Whenever a command is being executed, the Busy status bit is set. When a command is completed, an interrupt is generated and the Busy status bit is reset. The Status Register indicates whether the completed command encountered an error or was fault-free. For ease of discussion, commands are divided into four types. Commands and types are summarized in Table 2.

TYPE 1 COMMANDS

The Type 1 Commands include the RESTORE, SEEK, STEP, STEP-IN, and STEP-OUT commands. Each of the Type 1 Commands contain a rate field ($r_0 r_1$), which determines the stepping motor rate as defined in Table 1, page 4.

The Type 1 Commands contain a head load flag (h) which determines if the head is to be loaded at the beginning of the command. If h=1, the head is loaded at the beginning of the command (HLD output is made active). If h=0, HLD is deactivated. Once the head is loaded, the head will remain engaged until the FD1771 receives a command that specifically disengages the head. If the FD1771 does not receive any commands after two revolutions of the disk, the head will be automatically disengaged (HLD made inactive). The Head Load Timing Input is sampled after a 10 ms delay, when reading or writing on the disk is to occur.

The Type 1 Commands also contain a verification (V) flag which determines if a verification operation is to take place on the destination track. If V=1, a verification is performed; if V=0, no verification is performed.

During verification, the head is loaded and after an internal 10 ms delay, the HLT input is sampled. When

Table 2. COMMAND SUMMARY

		BITS							
TYPE	COMMAND	7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r_1	r_0
I	Seek	0	0	0	1	h	V	r_1	r_0
I	Step	0	0	1	u	h	V	r_1	r_0
I	Step In	0	1	0	u	h	V	r_1	r_0
I	Step Out	0	1	1	u	h	V	r_1	r_0
II	Read Command	1	0	0	m	b	E	0	0
II	Write Command	1	0	1	m	b	E	a_1	a_0
III	Read Address	1	1	0	0	0	E	0	0
III	Read Track	1	1	1	0	0	1	0	$\bar{s}$
III	Write Track	1	1	1	1	0	1	0	0
IV	Force Interrrupt	1	1	0	1	I_3	I_2	I_1	I_4

Note: Bits shown in TRUE form.

Table 3. FLAG SUMMARY

TYPE I

h = Head Load flag (Bit 3)
- h = 1, Load head at beginning
- h = 0, Do not load head at beginning

V = Verify flag (Bit 2)
- V = 1, Verify on last track
- V = 0, No verify

$r_1 r_0$ = Stepping motor rate (Bits 1-0)
- Refer to Table 1 for rate summary

u = Update flag (Bit 4)
- u = 1, Update Track register
- u = 0, No update

Table 4. FLAG SUMMARY

TYPE II

m = Multiple Record flag (Bit 4)
- m=0, Single Record
- m=1, Multiple Records

b = Block length flag (Bit 3)
- b=1, IBM format (128 to 1024 bytes)
- b=0, Non-IBM format (16 to 4096 bytes)

$a_1 a_0$ = Data Address Mark (Bits 1-0)
- $a_1 a_0$ = 00, FB (Data Mark)
- $a_1 a_0$ = 01, FA (User defined)
- $a_1 a_0$ = 10, F9 (User defined)
- $a_1 a_0$ = 11, F8 (Deleted Data Mark)

Table 5. FLAG SUMMARY

TYPE III

s = Synchronize flag (Bit 0)
- $\bar{s}$=0, Synchronize to AM
- $\bar{s}$=1, Do Not Synchronize to AM

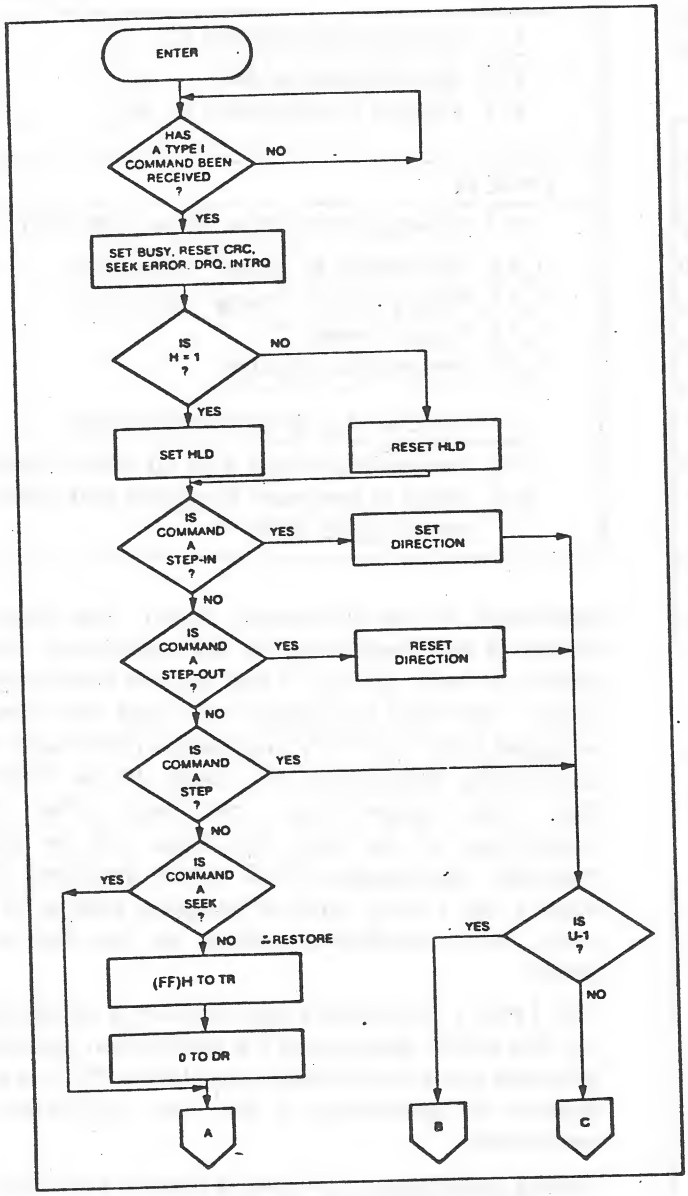
TYPE IV

Ii = Interrupt Condition flags (Bits 3-0)
- I_0=1, Not Ready to Ready Transition
- I_1=1, Ready to Not Ready Transition
- I_2=1, Index Pulse
- I_3=1, Immediate interrupt

E = Enable HLD and 10 msec Delay
- E=1, Enable HLD, HLT and 10 msec Delay
- E=0, Head is assumed Engaged and there is no 10 msec Delay

HLT is active (logic true), the first encountered ID field is read off the disk. The track address of the ID Field is then compared to the Track Register; if there is a match and a valid ID CRC, the verification is complete, an interrupt is generated and the BUSY status bit is reset. If there is not a match but there is valid ID CRC, an interrupt is generated, the Seek Error status bit (Status Bit 4) is set and the BUSY status bit is reset. If there is a match but not a valid CRC, the CRC error status bit is set (Status Bit 3), and the next encountered ID Field is read from the disk for the verification operation. If an ID Field with a valid CRC cannot be found after two revolutions of the disk, the FD1771 terminates the operation and sents an interrupt (INTRQ).

The STEP, STEP-IN, and STEP-OUT commands contain an UPDATE flag (U). When U=1, the track register is updated by one for each step. Whe U=0, the track register is not updated.



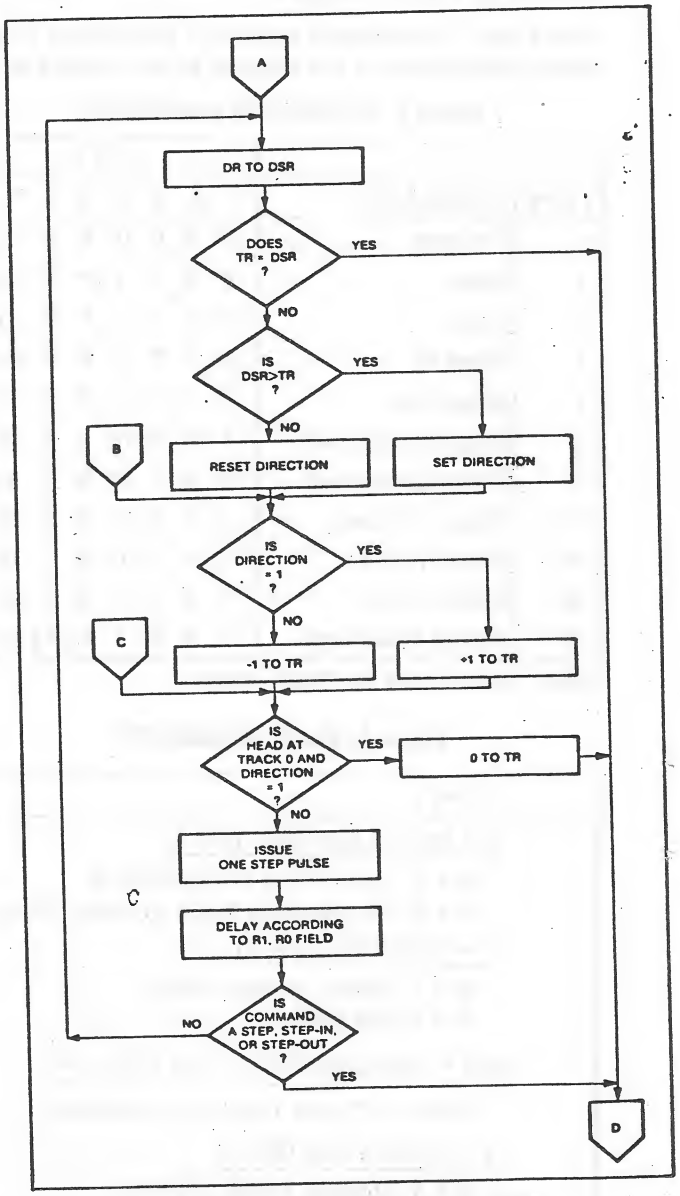
TYPE I COMMAND FLOW

RESTORE (SEEK TRACK 0)

Upon receipt of this command the Track 00 ($\overline{TR00}$) input is sampled. If $\overline{TR00}$ is active low indicating the Read-Write head is positioned over track 0, the Track Register is loaded with zeroes and an interrupt is generated. If $\overline{TR00}$ is not active low, stepping pulses (pins 15 to 17) at a rate specified by the r_1r_0 field are issued until the $\overline{TR00}$ input is activated. At this time the TR is loaded with zeroes and an interrupt is generated. If the $\overline{TR00}$ input does not go active low after 255 stepping pulses, the FD1771 terminates operation, interrupts, and sets the Seek error status bit. Note that the RESTORE command is executed when $\overline{MR}$ goes from an active to an inactive state. A verification operation takes place if the V flag is set. The h bit allows the head to be loaded at the start of command.

SEEK

This command assumes that the Track Register contains the track number of the current position of the

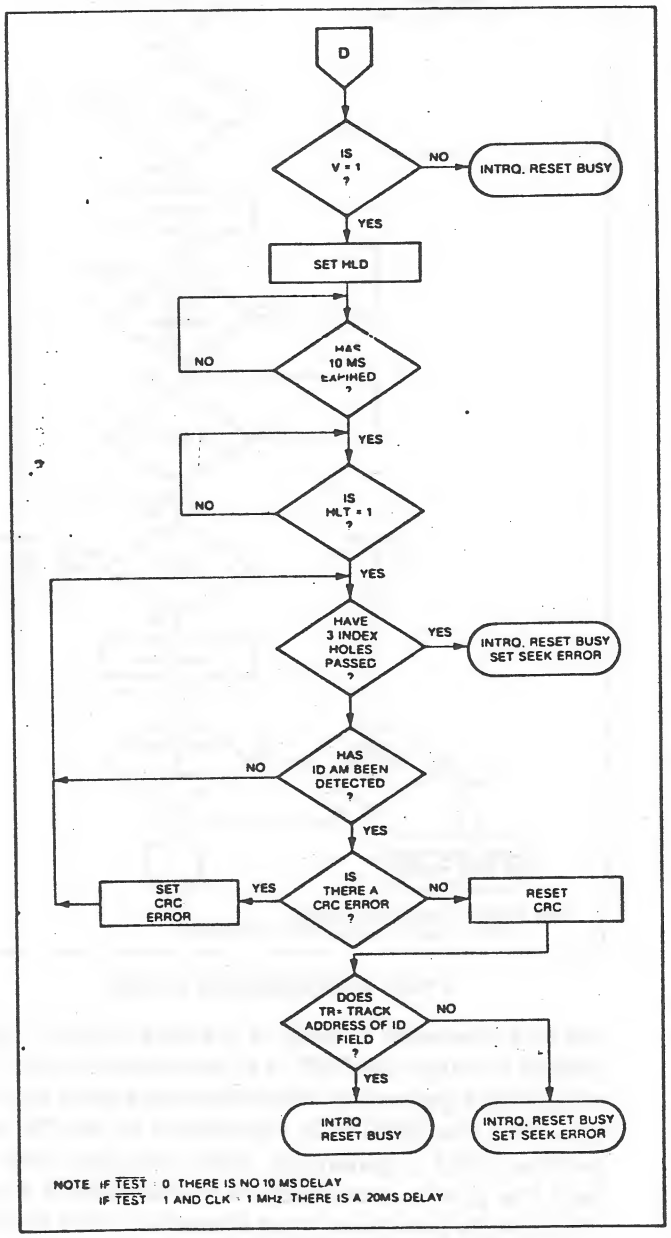


TYPE I COMMAND FLOW

Read-Write head and the Data Register contains the desired track number. The FD1771 will update the Track register and issue stepping pulses in the appropriate direction until the contents of the Track register are equal to the contents of the data register (the desired track location). A verification operation takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP

Upon receipt of this command, the FD1771 issues one stepping pulse to the disk drive. The stepping motor direction is the same as in the previous step command. After a delay determined by the r_1r_0 field, a verification takes place if the V flag is on. If the u flag is on, the TR is updated. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.



TYPE I COMMAND FLOW

STEP-IN

Upon receipt of this command, the FD1771 issues one stepping pulse in the direction towards track 76. If the u flag is on, the Track Register is incremented by one. After a delay determined by the r_1r_0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP-OUT

Upon receipt of this command, the FD1771 issues one stepping pulse in the direction towards track 0. If the u flag is on, the TR is decremented by one. After a delay determined by the r_1r_0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

TYPE II COMMANDS

The Type II Commands include the Read Sector(s) and Write Sector(s) commands. Prior to loading the Type II command into the COMMAND REGISTER, the computer must load the Sector Register with the desired sector number. Upon receipt of the Type II command, the Busy status bit is set. If the E flag=1 (this is the normal case), HLD is made active and HLT is sampled after a 10 msec delay. If the E flag is 0, the head is assumed to be engaged and there is no 10 msec delay. The ID field and the Data Field format are shown below.

When an ID field is located on the disk, the FD1771 compares the track number of the ID field with the Track Register. If there is not a match, the next encountered ID field is read and a comparison is again made. If there was a match, the Sector Number of the ID field is compared with the Sector Register. If there is not a Sector match, the next encountered ID field is read off the disk and comparisons again made. If the ID field CRC is correct, the data field is then located and will be either written into, or read from depending on the command. The FD1771 must find an ID field with a track number, Sector number, and CRC within two revolutions of the disk; otherwise, the Record Not Found status bit is set (Status bit 3) and the command is terminated with an interrupt.

Each of the Type II Commands contain a (b) flag which in conjunction with the sector length field contents of the ID determines the length (number of characters) of the Data field.

For IBM 3740 compatibility, the b flag should equal 1. The numbers of bytes in the data field (sector) is then 128×2^n where n = 0, 1, 2, 3.

GAP	ID AM	TRACK NUMBER	ZERO	SECTOR NUMBER	SECTOR LENGTH	CRC 1	CRC 2	GAP	DATA AM	DATA FIELD	CRC 1	CRC 2
ID FIELD									DATA FIELD			

IDAM = ID Address Mark — DATA = $(FE)_{16}$ CLK = $(C7)_{16}$

Data AM = Data Address Mark — DATA = (F8, F9, FA, or FB), CLK = $(C7)_{16}$

For b = 1

Sector Length Field (Hex)	Number of Bytes in Sector (Decimal)
00	128
01	256
02	512
03	1024

When the b flag equals zero, the sector length field (n) multiplied by 16 determines the number of bytes in the sector or data field as shown below.

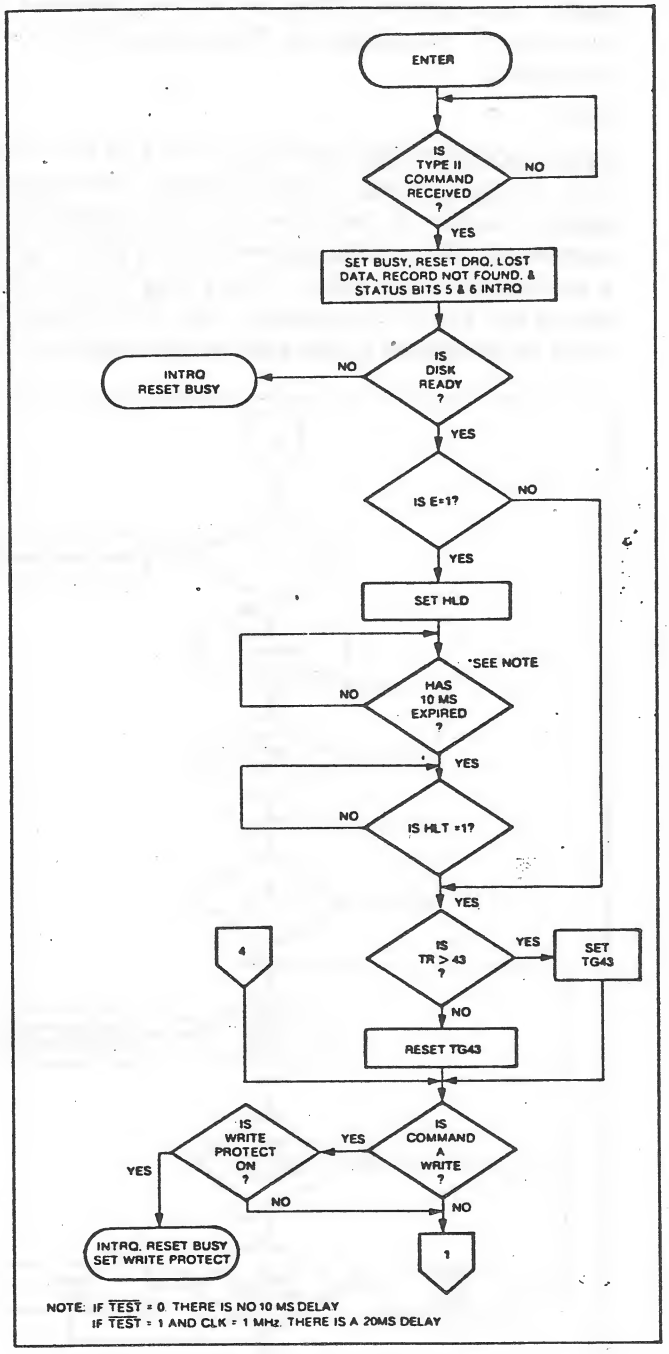
For b = 0

Sector Length Field (Hex)	Number of Bytes in Sector (Decimal)
01	16
02	32
03	48
04	64
•	•
•	•
•	•
FF	4080
00	4096

Each of the Type II commands also contain a (m) flag which determines if the multiple records (sectors) are to be read or written, depending upon the command. If m=0 a single sector is read or written and an interrupt is generated at the completion of the command. If m=1, multiple records are read or written with the sector register internally updated so that an address verification can occur on the next record. The FD1771 will continue to read or write multiple records and update the sector register until the sector register exceeds the number of sectors on the track or until the Force Interrupt command is loaded into the command register, which terminated the command and generates an interrupt.

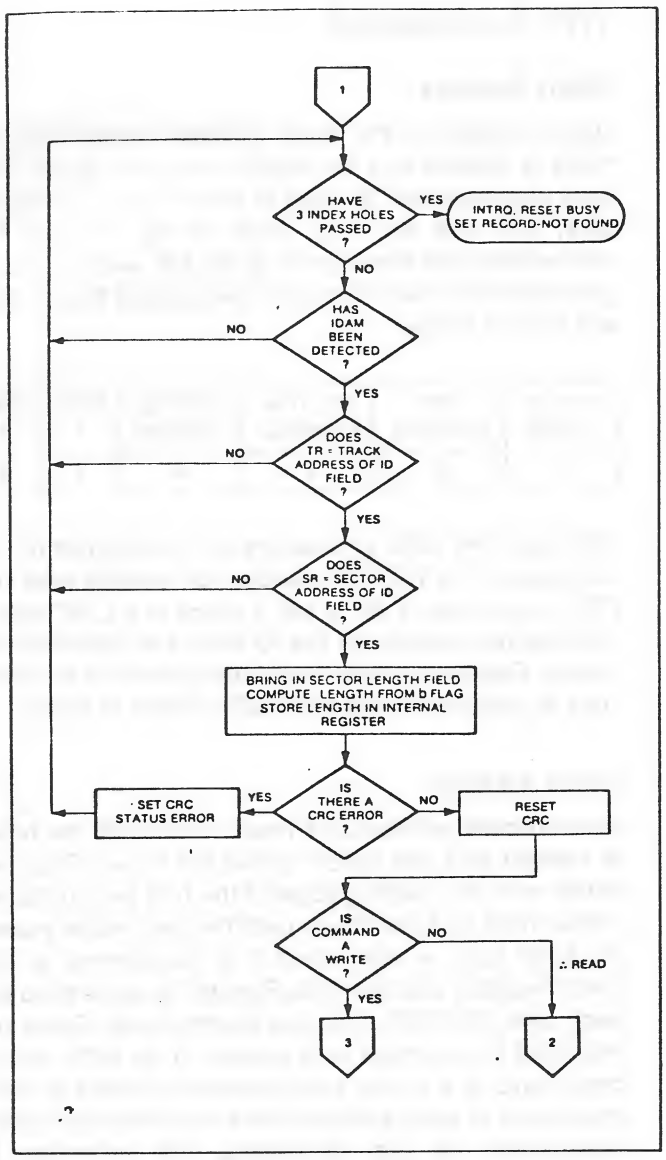
READ COMMAND

Upon receipt of the Read command, the head is loaded, the BUSY status bit set, and when an ID field is encountered that has the correct track number, correct sector number, and correct CRC, the data field is presented to the computer. The Data Address Mark of the data field must be found within 28 bytes of the correct field; if not, the Record Not Found status bit is set and the operation is terminated. When

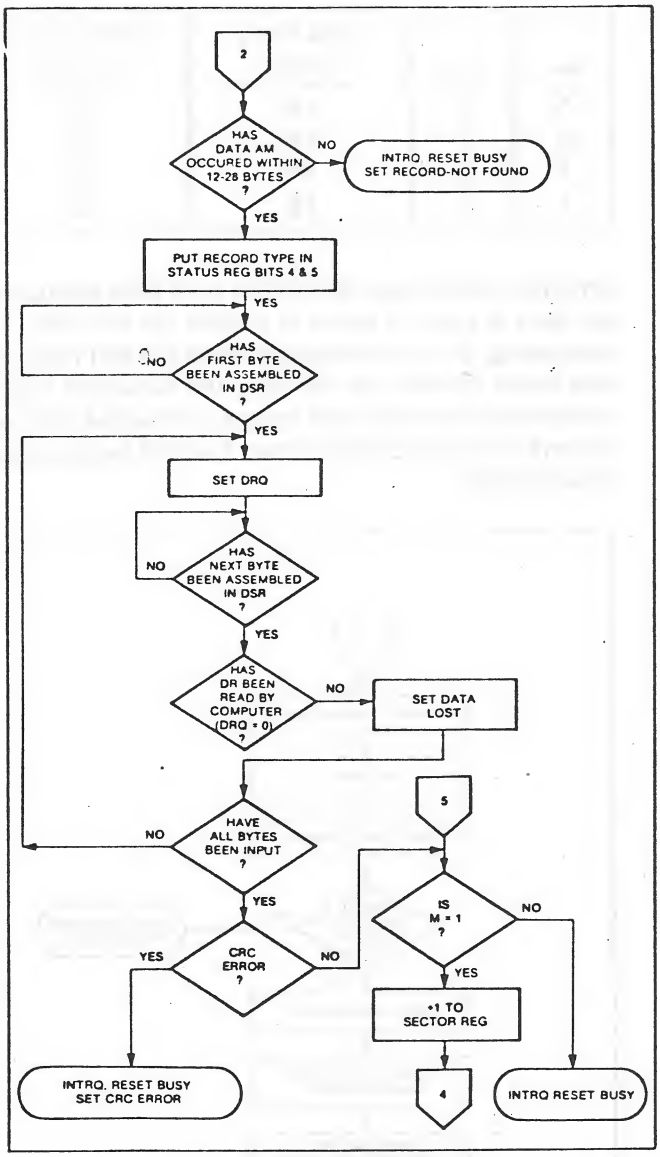


TYPE II COMMAND FLOW

the first character or byte of the data field has been shifted through the DSR, it is transferred to the DR, and DRQ is generated. When the next byte is accumulated in the DSR, it is transferred to the DR and another DRQ is generated. If the computer has not read the previous contents of the DR before a new character is transferred that character is lost and the



TYPE II COMMAND FLOW



TYPE II COMMAND FLOW

Lost Data status bit is set. This sequence continues until the complete data field has been input to the computer. If there is a CRC error at the end of the data field, the CRC error status bit is set, and the command is terminated (even if it is a mulltiple record command).

At the end of the Read operation, the type of Data Address Mark encountered in the data field is recorded in the Status Register (Bits 5 and 6) as shown below.

Status Bit 5	Status Bit 6	Data AM (Hex)
0	0	FB
0	1	FA
1	0	F9
1	1	F8

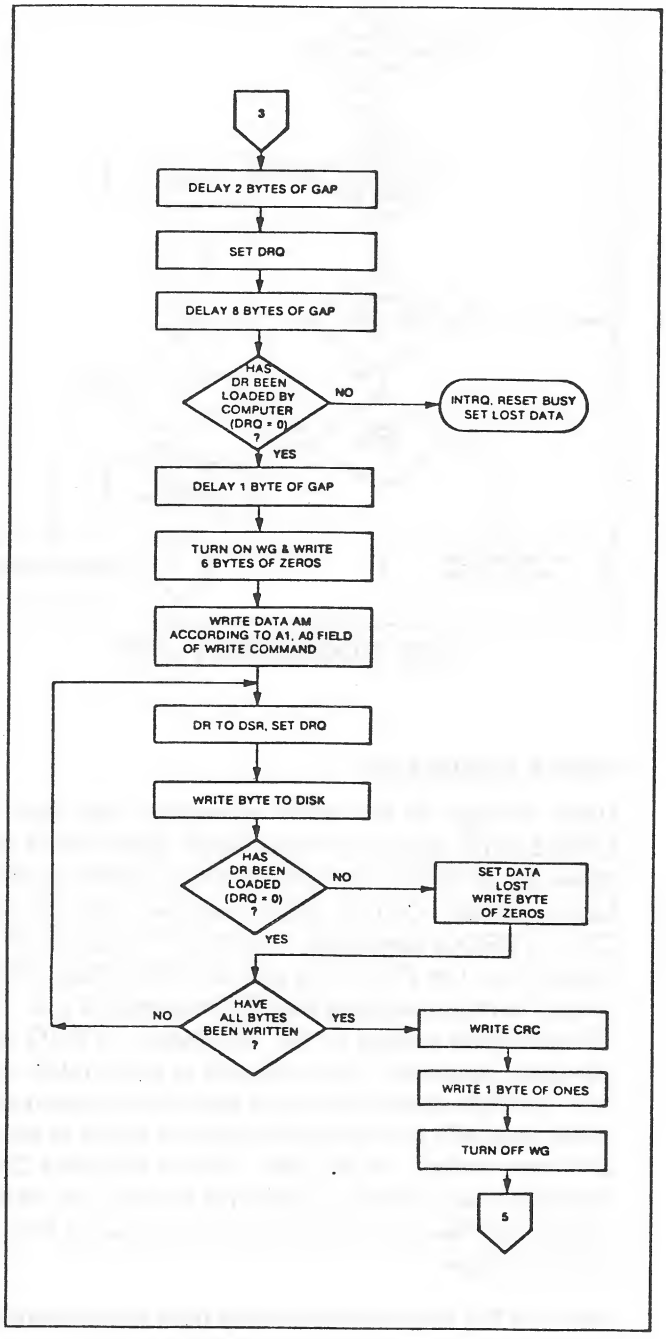
WRITE COMMAND

Upon receipt of the Write command, the head is loaded (HLD active) and the BUSY status bit is set. When an ID field is encountered that has the correct track number, correct sector number, and correct CRC, a DRQ is generated. The FD1771 counts off 11 bytes from the CRC field and the Write Gate (WG) output is made active if the DRQ is serviced (i.e., the DR has been loaded by the computer). If DRQ has not been serviced, the command is terminated and the Lost Data status bit is set. If the DRQ has been serviced, the WG is made active and six bytes of zeros are then written on the disk. At this time the Data Address Mark is then written on the disk as determined by the $a_1 a_0$ field of the command as shown on next page.

The FD1771 then writes the data field and generates DRQs to the computer. If the DRQ is not serviced in

a_1	a_0	Data Mark (Hex)	Clock Mark (Hex)
0	0	FB	C7
0	1	FA	C7
1	0	F9	C7
1	1	F8	C7

time for continuous writing the Lost Data status bit is set and a byte of zeros is written on the disk. The command is not terminated. After the last data byte has been written on the disk, the two-byte CRC is computed internally and written on the disk followed by one byte gap of logic ones. The WG output is then deactivated.



TYPE II COMMAND FLOW

TYPE III COMMANDS

READ Address

Upon receipt of the Read Address command, the head is loaded and the BUSY Status bit is set. The next encountered ID field is then read in from the disk, and the six data bytes of the ID field are assembled and transferred to the DR, and a DRQ is generated for each byte. The six bytes of the ID field are shown below.

TRACK ADDR	SIDE NUMBER	SECTOR ADDRESS	SECTOR LENGTH	CRC 1	CRC 2
1	2	3	4	5	6

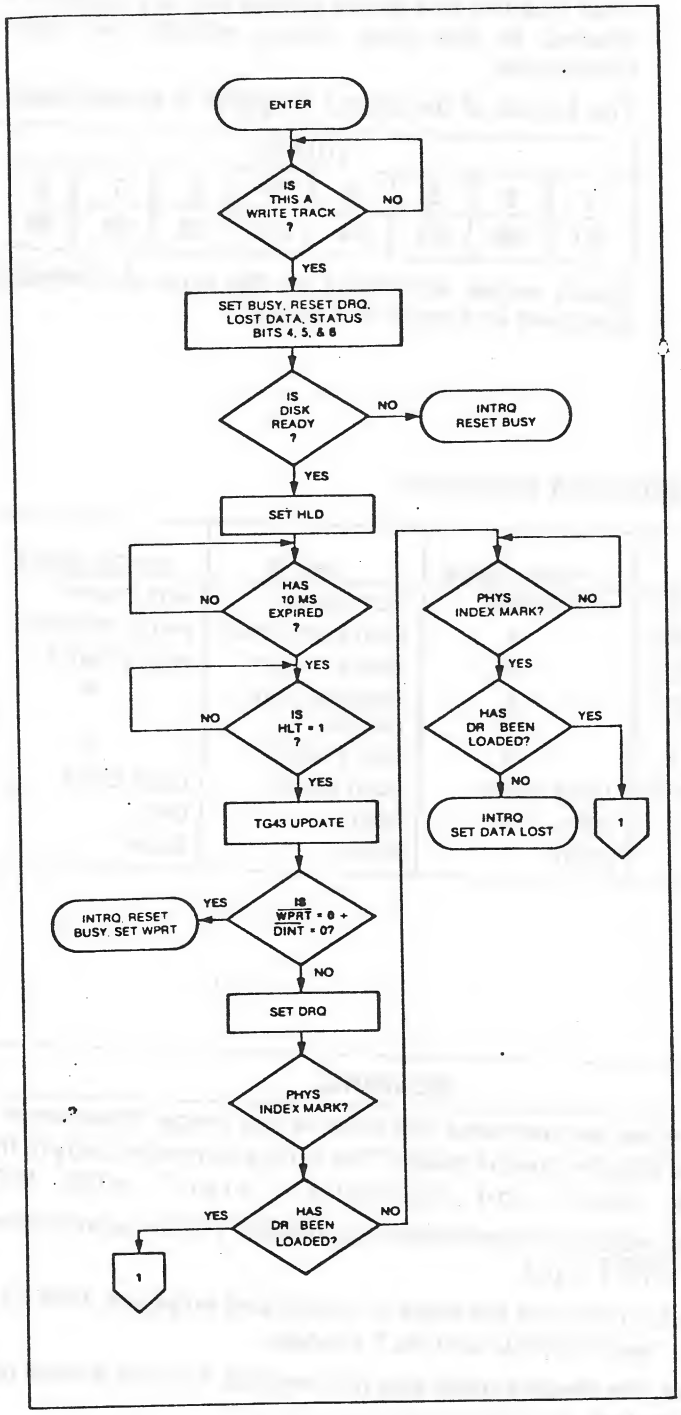
Although the CRC characters are transferred to the computer, the FD1771 checks for validity and the CRC error status bit is set if there is a CRC error. The Sector Address of the ID field is written into the Sector Register. At the end of the operation an interrupt is generated and the BUSY Status is reset.

READ TRACK

Upon receipt of the Read Track command, the head is loaded and the BUSY status bit is set. Reading starts with the leading edge of the first encountered index mark and continues until the next index pulse. As each byte is assembled it is transferred to the Data Register and the Data Request is generated for each byte. No CRC checking is performed. Gaps are included in the input data stream. If bit 0(S) of the command is a 0, the accumulation of bytes is synchronized to each Address Mark encountered. Upon completion of the command, the interrupt is activated.

WRITE TRACK

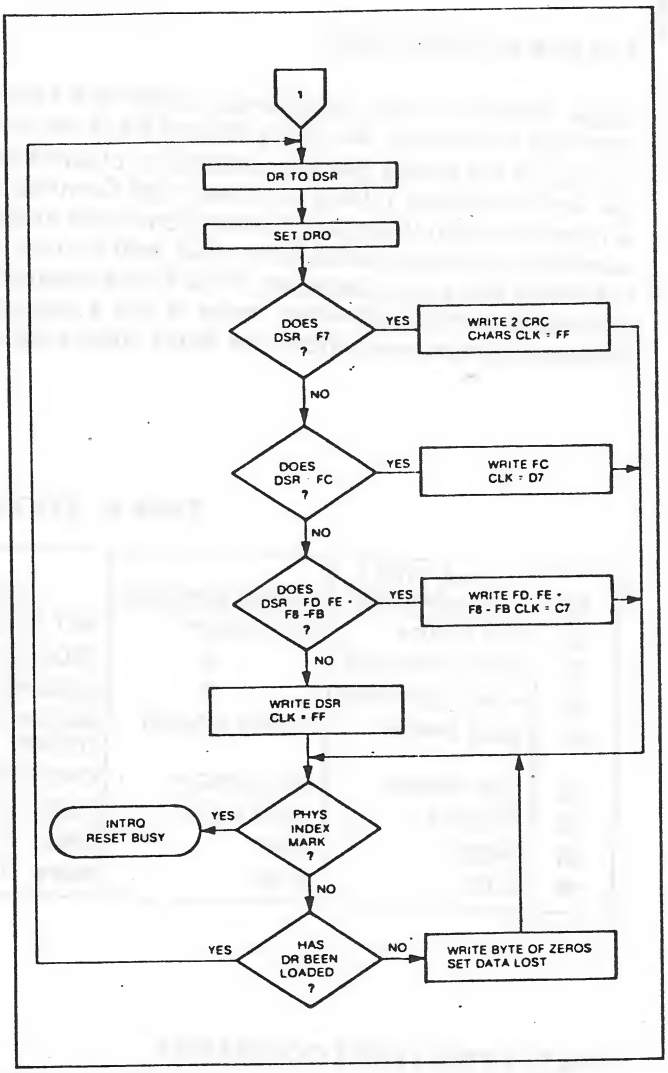
Upon receipt of the Write Track command, the head is loaded and the BUSY status bit is set. Writing starts with the leading edge of the first encountered index pulse and continues until the next index pulse, at which time the interrupt is activated. The Data Request is activated immediately upon receiving the command, but writing will not start until after the first byte has been loaded into the Data Register. If the DR has not been loaded by the time the index pulse is encountered the operation is terminated making the device Not Busy, the Lost Data status bit is set, and the Interrupt is activated. If a byte is not present in the DR when needed, a byte of zeros is substituted. Address Marks and CRC characters are written on the disk by detecting certain data byte patterns in the outgoing data stream as shown in the table below. The CRC generator is initialized when any data byte from F8 to FE is about to be transferred from the DR to the DSR.



TYPE III COMMAND WRITE TRACK

CONTROL BYTES FOR INITIALIZATION

DATA PATTERN (HEX)	INTERPRETATION	CLOCK MARK (HEX)
F7	Write CRC Character	FF
F8	Data Address Mark	C7
F9	Data Address Mark	C7
FA	Data Address Mark	C7
FB	Data Address Mark	C7
FC	Index Address Mark	D7
FD	Spare	
FE	ID Address Mark	C7



TYPE III COMMAND WRITE TRACK

The Write Track Command will not execute if the $\overline{DINT}$ input is grounded; instead, the Write Protect status bit is set and the interrupt is activated. Note that one F7 pattern generates two CRC characters.

TYPE IV COMMAND

Force Interrupt

This command can be loaded into the command register at any time. If there is a current command under execution (BUSY status bit set), the command will be terminated and an interrupt will be generated when the condition specified in the I_0 through I_3 field is detected. The interrupt conditions are shown below:

I_0= Not-Ready-To-Ready Transition
I_1 = Ready-To-Not-Ready Transition
I_2 = Every Index Pulse
I_3 = Immediate Interrupt (Requires reset, see Note)

NOTE: If $I_0 - I_3 = 0$, there is no interrupt generated but the current command is terminated and busy is reset. This is the only command that will clear the immediate interrupt.

STATUS DESCRIPTION

Upon receipt of any command, except the Force Interrupt command, the Busy Status bit is set and the rest of the status bits are updated or cleared for the new command. If the Force Interrupt Command is received when there is a current command under execution, the Busy status bit is reset, and the rest of the status bits are unchanged. If the Force Interrupt command is received when there is not a current command under execution, the Busy Status bit is reset and the rest of the status bits are updated or cleared. In this case, Status reflects the Type I commands.

The format of the Status Register is shown below.

(BITS)							
7	6	5	4	3	2	1	0
S7	S6	S5	S4	S3	S2	S1	S0

Status varies according to the type of command executed as shown in Table 6.

Table 6. STATUS REGISTER SUMMARY

BIT	ALL TYPE I COMMANDS	READ ADDRESS	READ	READ TRACK	WRITE	WRITE TRACK
S7	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY
S6	WRITE PROTECT	0	RECORD TYPE	0	WRITE PROTECT	WRITE PROTECT
S5	HEAD ENGAGED	0	RECORD TYPE	0	WRITE FAULT	WRITE FAULT
S4	SEEK ERROR	ID NOT FOUND	RECORD NOT FOUND	0	RECORD NOT FOUND	0
S3	CRC ERROR	CRC ERROR	CRC ERROR	0	CRC ERROR	0
S2	TRACK 0	LOST DATA	LOST DATA	LOST DATA	LOST DATA	LOST DATA
S1	INDEX	DRQ	DRQ	DRQ	DRQ	DRQ
S0	BUSY	BUSY	BUSY	BUSY	BUSY	BUSY

STATUS FOR TYPE I COMMANDS

BIT	NAME	MEANING
S7	NOT READY	This bit when set indicates the drive is not ready. When reset it indicates that the drive is ready. This bit is an inverted copy of the READY input and logically "ored" with MR.
S6	PROTECTED	When set, indicates Write Protect is activated. This bit is an inverted copy of $\overline{WRPT}$ input.
S5	HEAD LOADED	When set, it indicates the head is loaded and engaged. This bit is a logical "and" of HLD and HLT signals.
S4	SEEK ERROR	When set, the desired track was not verified. This bit is reset to 0 when updated.
S3	CRC ERROR	When set, there was one or more CRC errors encountered on an unsuccessful track verification operation. This bit is reset to 0 when updated.
S2	TRACK 00	When set, indicates Read-Write head is positioned to Track 0. This bit is an inverted copy of the $\overline{TR00}$ input.
S1	INDEX	When set, indicates index mark detected from drive. This bit is an inverted copy of the IP input.
S0	BUSY	When set,command is in progress. When reset, no command is in progress.

STATUS BITS FOR TYPE II AND III COMMANDS

BIT	NAME	MEANING
S7	NOT READY	This bit when set indicates the drive is not ready. When reset, it indicates that the drive is ready. This bit is an inverted copy of the READY input and "ored" with MR. The TYPE II and III Commands will not execute unless the drive is ready.
S6	RECORD TYPE/WRITE PROTECT	On Read Record: It indicates the MSB of record-type code from data field address mark. On Read Track: Not Used. On any Write Track: It indicates a Write Protect. This bit is reset when updated.
S5	RECORD TYPE/WRITE FAULT	On Read Record: It indicates the LSB of record-type code from data field address mark. On Read Track: Not Used. On any Write Track: It indicates a Write Fault. This bit is reset when updated.
S4	RECORD NOT FOUND	When set, it indicates that the desired track and sector were not found. This bit is reset when updated.
S3	CRC ERROR	If S4 is set, an error is found in one or more ID fields; otherwise it indicates error in data field. This bit is reset when updated.
S2	LOST DATA	When set, it indicates the computer did not respond to DRQ in one byte time. This bit is reset to zero when updated.
S1	DATA REQUEST	This bit is a copy of the DRQ output. When set, it indicates the DR is full on a Read operation or the DR is empty on a Write operation. This bit is reset to zero when updated.
S0	BUSY	When set, command is under execution. When reset, no command is under execution.

FORMATTING THE DISK (Refer to section on Type III Commands for flow diagrams.)

Formatting the disk is a relatively simple task when operating programmed I/O or when operating under DMA control with a large amount of memory. When operating under DMA with limited amount of memory, formatting is a more difficult task. This is because gaps as well as data must be provided at the computer interface.

Formatting the disk is accomplished by positioning the R/W head over the desired track number and issuing the Write Track command. Upon receipt of the Write Track command, the FD1771 raises the Data Request signal. At this point in time, the user loads the Data Register with desired data to be written on the disk. For every byte of information to be written on the disk, a Data Request is generated. This sequence continues from one index mark to the next index mark. Normally, whatever data pattern appears in the Data Register is written on the disk with a clock mark of $(FF)_{16}$. However, if the FD1771 detects a data pattern on F7 through FE in the Data Register, this is interpreted as data address marks with missing clocks or CRC generation. For instance, an FE pattern will be interpreted as an ID address mark (DATA-FE, CLK-C7) and the CRC will be initialized. An F7 pattern will generate two CRC characters. As a consequence, the patterns F7 through FE must not appear in the gaps, data fields, or ID fields. Also, CRCs must be generated by an F7 pattern.

Disks may be formatted in IBM 3740 formats with sector lengths of 128,256,512, or 1024 bytes, or may be formatted in non-IBM format with sector lengths of 16 to 4096 bytes in 16-byte increments. IBM 3740 at the present time only defines two formats. One format with 128 bytes/sector and the other with 256 bytes/sector. The next section deals with the IBM 3740 format with 128 bytes/sector followed by a section of non-IBM formats.

IBM 3740 Formats — 128 Bytes/Sector

The IBM format with 128 bytes/sector is depicted in the Track Format figure on the following page. In order to create this format, the user must issue the

Write Track command, and load the data register with the following values. For every byte to be written, there is one data request.

Number of Bytes	Hex Value of Byte Written
40	00 or FF
6	00
1	FC (Index Mark)
* 26	00 or FF
6	00
1	FE (ID Address Mark)
1	Track Number (0 through 4C)
1	00
1	Sector Number (1 through 1A)
1	00
1	F7 (two CRCs written)
11	00 or FF
6	00
1	FB (Data Address Mark)
128	Data (IBM uses E5)
1	F7 (two CRCs written)
27	00 or FF
247 **	00 or FF

*Write bracketed field 26 times.

**Continue writing until FD1771 interrupts out. Approximately 247 bytes.

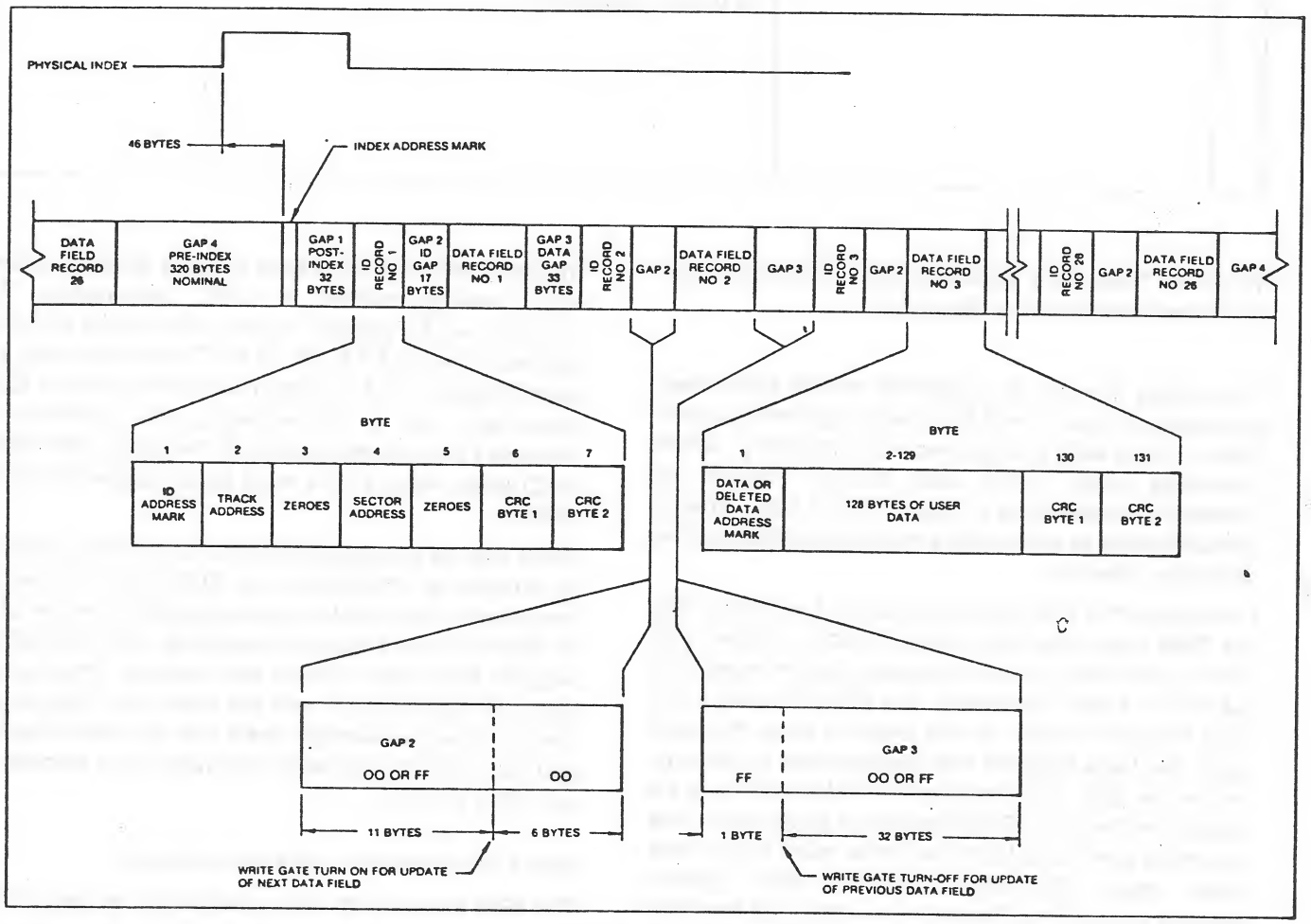
Non-IBM Formats

Non-IBM formats are very similar to the IBM formats except a different algorithm is used to ascertain the sector length from the sector length byte in the ID field. This permits a wide range of sector lengths from 16 to 4096 bytes. Refer to Section V, Type II commands with b flag equal to zero. Note that F7 through FE must not appear in the sector length byte of the ID field.

In formatting the FD1771, only two requirements regarding GAP sizes must be met. GAP 2 (i.e., the gap between the ID field and data field) must be 17 bytes of which the last 6 bytes must be zero and that every address mark be preceded by at least one byte of zeros. However, it is recommended that every GAP be at least 17 bytes long with 6 bytes of zeros. The FD1771 does not require the index address mark (i.e., DATA = FC, CLK = D7) and need not be present.

References:

1) IBM Diskette OEM Information GA21-9190-1.
2) SA900 IBM Compatibility Reference Manual — Shugart Associates.



TRACK FORMAT

ELECTRICAL CHARACTERISTICS

Maxium Ratings

V_{DD} with respect to V_{BB} (Ground)	+20 to -0.3V
Max Voltage to any input with respect to V_{BB}	+20 to -0.3V
Operating Temperature	0° C to 70° C
Storage Temperature	-55° C to +125° C

OPERATING CHARACTERISTICS (DC)

T_A = 0° C to 70° C, V_{DD} = +12.0V ± .6V,
V_{BB} = -5.0 ± .5V, V_{SS} = 0V, V_{CC} = +5V ± .25V
I_{DD} = 10 ma Nominal, I_{CC} = 30 ma Nominal,
I_{BB} = 0.4 μa Nominal

Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
I_{LI}	Input Leakage			10	μA	$V_{IN} = V_{DD}$
I_{LO}	Output Leakage			10	μA	$V_{OUT} = V_{DD}$
V_{IH}	Input High Voltage	2.6			V	
V_{IL}	Input Low Voltage (All Inputs)			0.8	V	
V_{OH}	Output High Voltage	2.8			V	I_O = -100 uA
V_{OL}	Output Low Voltage			0.45**	V	I_O = 1.0 mA

**Write Gate $V_{OL} \leq$ 0.5V.

TIMING CHARACTERISTICS

TA = 0° C to 70° C, V_{DD} = +12V ± .6V,
V_{BB} = -5V ± .25V, V_{SS} = 0V, V_{CC} = +5V ± .25V

NOTE: Timings are given for 2 MHz Clock. For those timings noted, values will double when chip is operated at 1 MHz. Use 1 MHz when using mini-floppy.

Read Operations

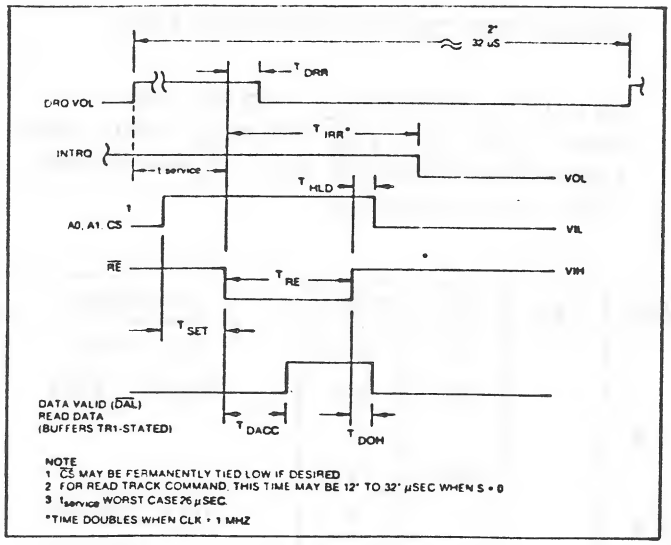
Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
TSET	Setup ADDR and CS to $\overline{RE}$	100			nsec	
THLD	Hold ADDR and CS from $\overline{RE}$	10			nsec	
TRE	$\overline{RE}$ Pulse Width	500			nsec	C_L = 25 pf
TDRR	DRQ Reset from $\overline{RE}$			500	nsec	
TIRR	INTRQ Reset from $\overline{RE}$			3000	nsec	
TDACC	Data Access from $\overline{RE}$			450	nsec	C_L = 25 pf
TDOH	Data Hold from $\overline{RE}$	50		150	nsec	C_L = 25 pf

Write Operations

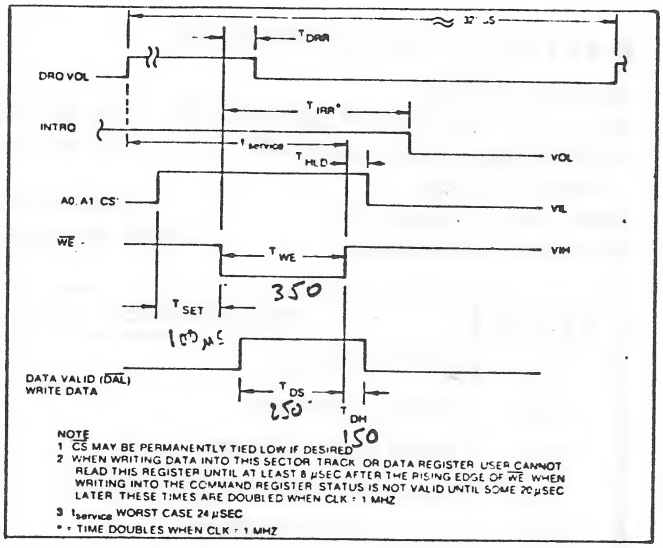
Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
TSET	Setup ADDR and CS to $\overline{WE}$	100			nsec	
THLD	Hold ADDR and CS from $\overline{WE}$	10			nsec	
TWE	$\overline{WE}$ Pulse Width	350			nsec	
TDRR	DRQ Reset from $\overline{WE}$			500	nsec	
TIRR	INTRQ Reset from $\overline{WE}$			3000	nsec	See Note
TDS	Data Setup to $\overline{WE}$	250			nsec	
TDH	Data Hold from $\overline{WE}$	150			nsec	

External Data Separation ($\overline{XTDS}$ = 0)

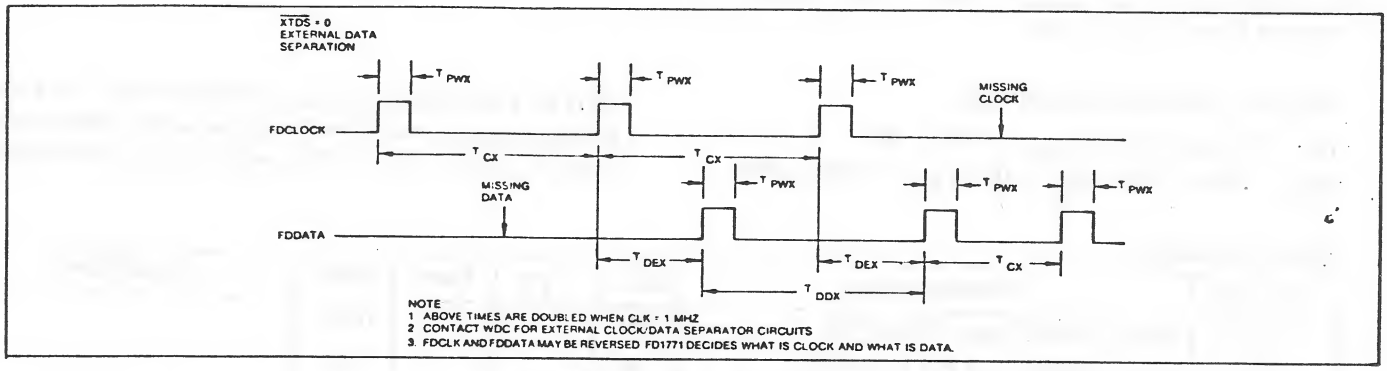
Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
TPWX	Pulse Width Read Data & Read Clock	150		350	nsec	
TCX	Clock Cycle External	2500			nsec	
TDEX	Data to Clock	500			nsec	
TDDX	Data to Data Cycie	2500			nsec	



READ ENABLE TIMING



WRITE ENABLE TIMING



READ TIMING ($\overline{XTDS}$ = 0)

Internal Data Separation ($\overline{XTDS}$ = 1)

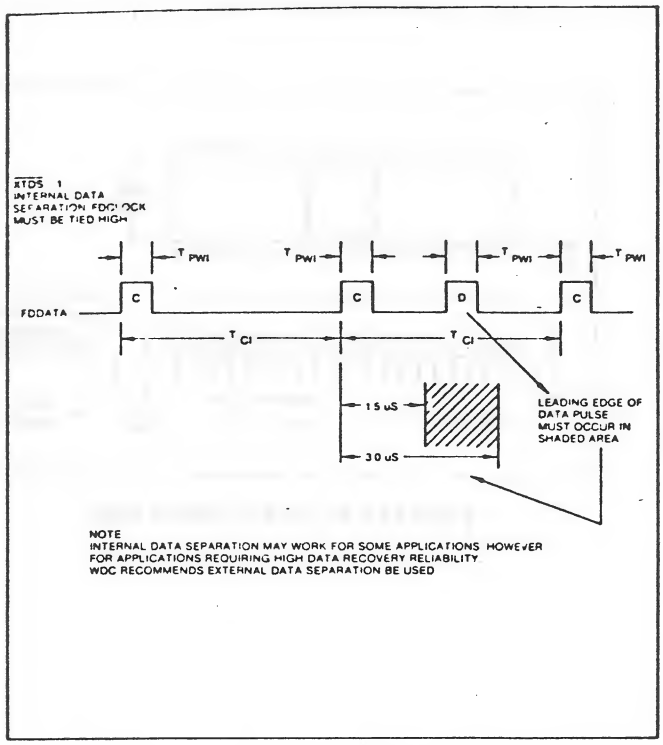
Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
TPWI	Pulse Width Data and Clock	150		1000	nsec	
TCI	Clock Cycle Internal	3500		5000	nsec	

Write Data Timing

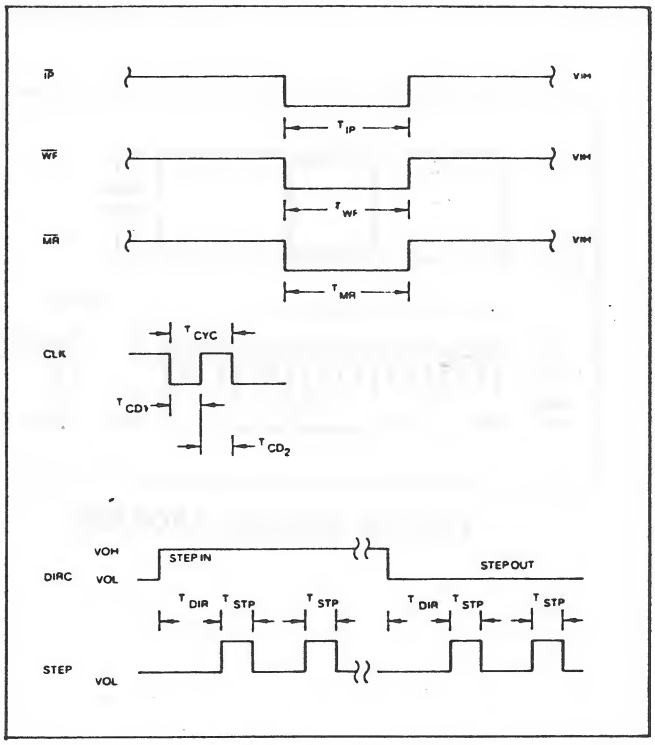
Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
TWGD	Write Gate to Data		1200		nsec	300 nsec ± CLK tolerance
TPWW	Pulse Width Write Data	500		600	nsec	
TCDW	Clock to Data		2000		nsec	± CLK tolerance
TCW	Clock Cycle Write		4000		nsec	± CLK tolerance
TWGH	Write Gate Hold to Data	0		100	nsec	

Miscellaeous Timing

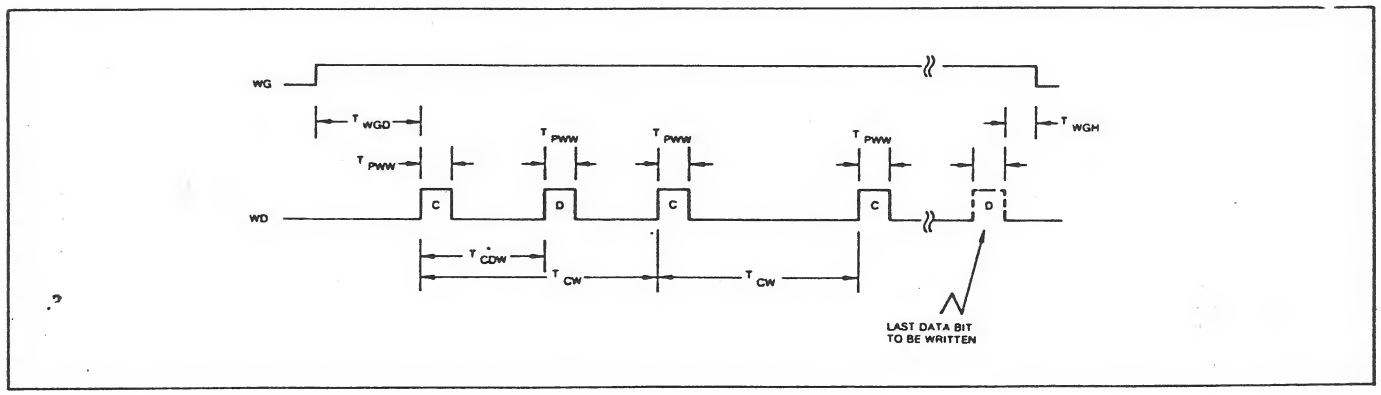
Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
TCD_1	Clock Duty	175			nsec	2 MHz ± 1% See Note
TCD_2	Clock Duty	210			nsec	
TSTP	Step Pulse Output	3800		4200	nsec	These times doubled when CLK = 1 MHz
TDIR	Direct Setup to Step	24			usec	
TMR	Master Reset Pulse Width	10			usec	
TIP	Index Pulse Width	10			usec	
TWF	Write Fault Pulse Width	10			usec	



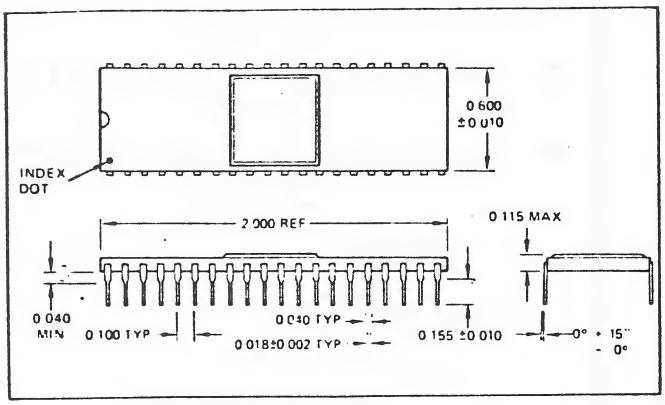
READ TIMING ($\overline{XTDS}$ = 1)



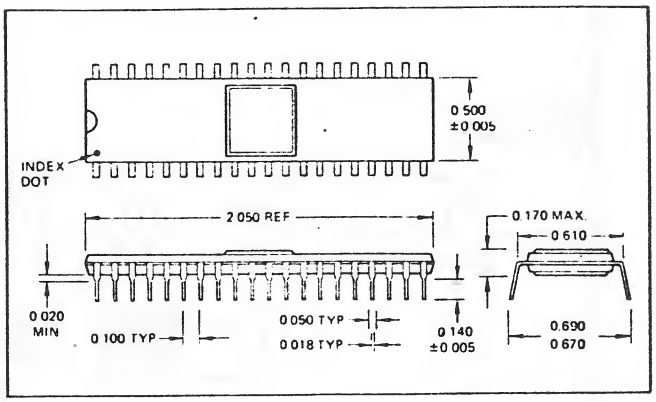
MISCELLANEOUS TIMING



WRITE DATA TIMING



FD1771A CERAMIC PACKAGE



FD1771B PLASTIC PACKAGE

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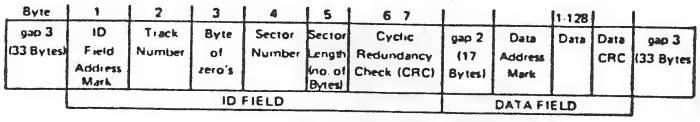
FLOPPY DISK CONTROLLER APPLICATION NOTE

Introduction

The FD1771 is a MOS/LSI device that performs the function of interfacing a processor to a flexible (Floppy) diskette drive. This single chip replaces nearly 80% of the required disk drive interface electronics. (See figure 1-1). It provides the data accessing controls and the bidirectional transfer of information between the processor's memory and the magnetically stored data on the diskette. The diskette data is stored in a data entry format compatible with the IBM 3740 specification (other formats may be used providing more data storage). In this format all information is recorded on tracks (radial paths) in sectors (arc sections) defined by a programmed header as shown below:



The FD1771 handles single density frequency modulated (FM) data. Each data cell is defined by clock pulses. A pulse recorded between clock pulses identifies the presence of a logic 1 bit; the absence of this pulse is interpreted as a logic 0 bit. The Address Marks for Index, ID, and Data are identified by a particular pattern not repeated in the remainder of the ID field or Data field. This is accomplished by reading patterns that are recorded with missing clock bits (logic 0) as shown below:

Index Address Mark	Data	1 1 1 1 1 1 0 0	=FC
	Clock	1 1 0 1 0 1 1 1	=D7
ID Address Mark	Data	1 1 1 1 1 1 1 0	=FE
	Clock	1 1 0 0 0 1 1 1	=C7
Data Address Mark	Data	1 1 1 1 1 0 1 1	=FB
	Clock	1 1 0 0 0 1 1 1	=C7
Deleted Data Address Mark	Data	1 1 1 1 1 0 0 0	=F8
	Clock	1 1 0 0 0 1 1 1	=C7

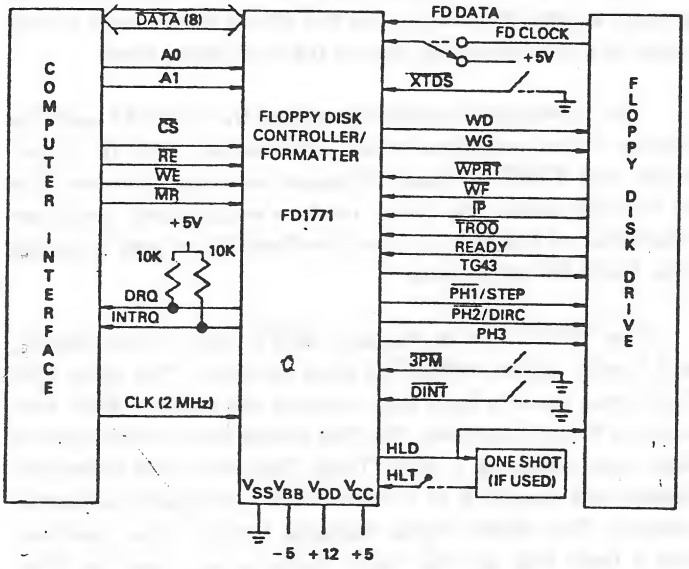
These patterns are used as synchronization codes by the FD1771 when reading data and are recorded by the formatting command, Write Track, when the FD1771 is presented with data F7 through FE.

SECTION I FD1771 DESCRIPTION

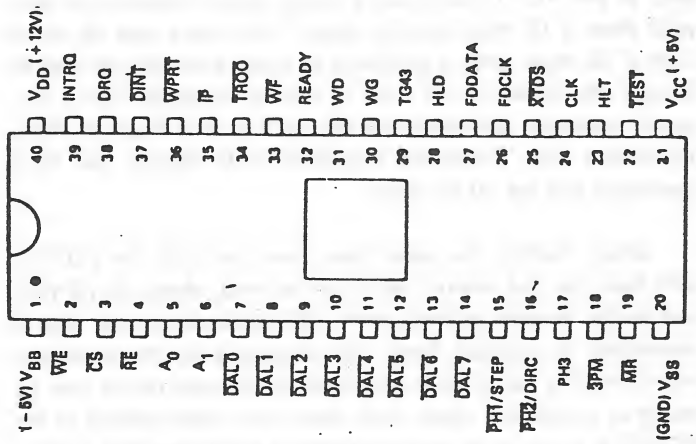
1.1 FD1771 — Flexible Drive Interface (Refer to Figure 1-1 FD1771 Block Diagram)

The FD1771 generates all controls to position the read/write head over the desired track. The FD1771 has the capability of sending successive three phase pulses over the lines PH1, PH2, and PH3 for 3 phase stepping motors or by sending a level over the PH2 line and pulses over the PH1 lines to determine direction and stepping rate for step-direction motors. The particular motor interface is chosen by hardwiring the external pin, 3PM.

ALL REFERENCE TO FD1771 DENOTES FD1771-01 VERSION



FD1771 SYSTEM BLOCK DIAGRAM
FIG 1



A Suffix = Ceramic
B Suffix = Plastic

FD1771 PIN CONNECTIONS
FIG 2

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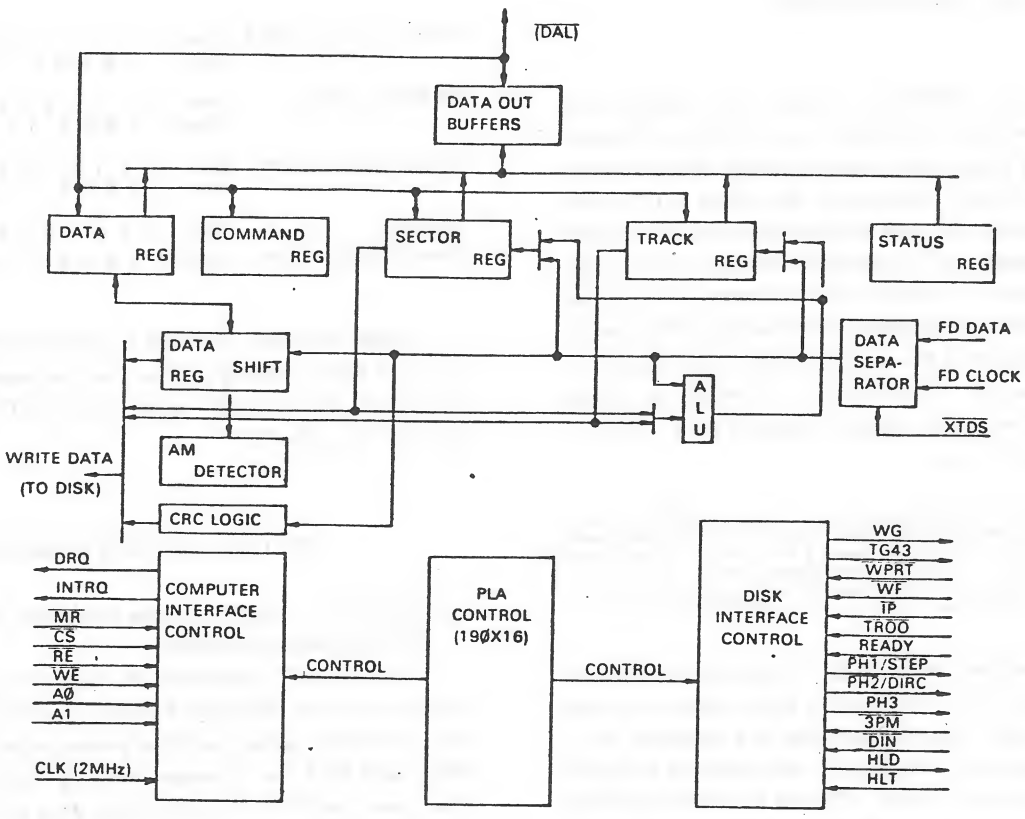

FIGURE 1-1

The head is loaded against the recording media (diskette) by the HLD (Head Load) signal from the FD1771. A read or write operation does not occur until a logic high signal is sampled at the HLT (Head Load Timing) input. This input is sampled after a 10 msec internal delay. This input may be wired high if 10 msec time is sufficient or a one shot may be used to extend this time. If the head is already engaged from a previous operation the resetting of bit 2 in the Read or Write Command (see Processor Interface) will disable the HLT functions and the 10 ms delay.

When reading the serial data from the disk the FD1771 will look for the desired sector to be read, check its ID field and locate its data address mark. All subsequent serial data is assembled in parallel form and presented to the processor interface. The serial data read from the Floppy Driver may be input as composite data, both clock and data present at the FDDATA input, or as separated data in which the data is input to the FDDATA pin and the clock is input to the FD Clock pin.

When writing, information is presented as composite of serial clock and data pulses of 500 nsec periods. With data present at the WD output the WG (Write Gate) signal is activated to allow current to flow in the Read/Write head.

The remaining interface between the FD1771 and the Floppy Drive concerns status information. The $\overline{IP}$ (Index Pulse) and $\overline{TROO}$ (Track 00) signals are outputs of the drive to indicate when the index mark is encountered (once per revolution of the disk) or when the Read/Write head is located over Track 00 respectively.

The $\overline{WPRT}$ (Write Protect), $\overline{DINT}$ (Disk Initialization), and Ready signals reflect the drive condition. The Write Protect signal, when a logic low, prevents the FD1771 from executing a Write Command. The Disk Initialization input, when a logic low, prevents a Write Track Command and essentially disables the rewriting of a format over a previously formatted diskette. The Ready signal indicates Floppy Drive readiness and a logic low on this input prevents any Read or Write command from being exeouted.

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Other status interface signals are $\overline{WF}$ (Write Fault) from the Drive which signifies a write operation fault such as failure to detect write current when WG is turned on terminating the Current Write command; and the TG43 signal to the drive indicating the track to be written on is located between Track 44 and Track 76. This latter signal is used by the drive to lower the write current on inner tracks and compensate for the higher density recording of these tracks.

1.2 FD1771 — Processor Interface (See figure 1-1)

All commands, status and data are transferred over the 3 state bidirectional $\overline{DAL}$ (Data Access) lines. These 8 lines present an open circuit to the common processor peripheral bus until activated by the $\overline{CS}$ (Chip Select) signal. An active $\overline{CS}$ combined with $\overline{RE}$ (Read Enable) sets the $\overline{DAL}$ into the transmitter mode while the $\overline{CS}$ combined with an active WE (Write Enable) sets the $\overline{DAL}$ in the receiver mode. The information in the FD1771 resides in 5 accessible 8 bit registers. These registers are: (1) The bidirectional Data Register which acts as a parallel buffer for read or write operations, and receives the desired track number to be accessed in seek operation. (2) the Command register which receives and stores commands from the processor, (3) The sector register which receives the desired sector number to be accessed, (4) The track register which contains the present Track position, (5) The Status Register containing information about the present operation.

The accessing of the registers is accomplished by a combination of active levels on the $\overline{CS}$, $\overline{RE}$, or $\overline{WE}$, and the register address lines A1 and A0. The Command Register can only receive information and the Status Register can only transmit information.

Two signals are available to aid in program response to the FD1771. The INTRQ (Interrupt Request) is activated by the controller whenever an operation is completed successfully or terminated by a fault. The DRQ (Data Request) signal is available as an indication of the chips readiness to transfer a byte of data during read or write operations.

A 2MHZ clock is required by the chip as a reference for all timed signals such as motor controls and data transfers. The $\overline{MR}$ (Master Reset) clears the command register and initiates a Restore (seek track 00) Command when the $\overline{MR}$ line is returned to an inactive state.

1.3 FD1771 Instructions

The FD1771 can be considered a specialized microprocessor with its own instruction repertoire. These are listed in the Tables below.

The Restore, Seek, and the three Step commands position the Read/Write head over the desired track. The Restore positions it over Track 00, the Seek poisitions it over the track specified in the Data Register, and the Step Commands position the head over an adjacent track to its present position.

The Step In moves the head inward toward the center of the disk while the Step Out moves it outward from the center. The Step Command moves the head one step in the same direction as the previous command.

The Read and Write commands are the normally executed commands when transferring information. The Read command initiates a search for a track and sector code in the ID field equal to that in the track and sector registers. When found, the data is formatted from serial to parallel and presented to the Data Register along with the setting of the DRQ signal. By setting of bit 4 in the Read (or Write) command all data records from the desired sector until the last sector on the track are sequentially assembled. The setting of bit 3 allows other combinations of byte count per sector than the standard IBM format.

The Write Command operates similar to the Read Command in multiple sector and variable sector length. All received words in the Data register are transferred to the shift register at which time the DRQ line is set. Four separate Data address marks are selectable through bits 1 and 0 which are written on the diskette prior to writing the sector data.

The Read Address command provides the next encountered ID field (6 bytes) on the diskette to the processor. This can be used to identify the track over which the head resides and can be used if one were to multiplex between two or more drives and wish to return to the first drive. This could also be accomplished by storing the track register in memory and returning it when reactivating the first drive.

The Write Track command is basically used for formatting. Once the index position is located the FD1771 will request data and transfer it to the disk including all ID fields, gaps, and Data fields. Special address marks and the CRC characters are written by detecting certain data patterns. The Read track command allows the reading of the entire recorded pattern on a track including gaps. (Refer to Data Sheet for formatting details)

The final command is the Force interrupt which can be loaded into the Command register at any time. This will terminate any present operation and can also generate an interrupt under four selectable conditions.

1.4 Status Register (See Table 1, page 16)

This register contains status information associated with each of the command instructions. Bit 7 always reflects the Ready condition of the Drive while bit 0 (Busy) always defines the status of the FD1771 concerning present operations.

COMMAND SUMMARY

		BITS							
TYPE	COMMAND	7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r_1	r_0
I	Seek	0	0	0	1	h	V	r_1	r_0
I	Step	0	0	1	u	h	V	r_1	r_0
I	Step In	0	1	0	u	h	V	r_1	r_0
I	Step Out	0	1	1	u	h	V	r_1	r_0
II	Read Command	1	0	0	m	b	E	0	0
II	Write Command	1	0	1	m	b	E	a_1	a_0
III	Read Address	1	1	0	0	0	1	0	0
III	Read Track	1	1	1	0	0	1	0	$\bar{s}$
III	Write Track	1	1	1	1	0	1	0	0
IV	Force Interrupt	1	1	0	1	I_3	I_2	I_1	I_0

COMMAND FLAG SUMMARY

TYPE I

h = Head Load flag (Bit 3)

h=1, Load head at beginning
h=0, Do not load head at beginning

V = Verify flag (Bit 2)

V=1, Verify on last track
V=0, No verify

r_1r_0 = Stepping motor rate (Bits 1-0)

r_1r_0=00, 6ms between steps
r_1r_0=01, 6 ms between steps
r_1r_0=10, 10ms between steps
r_1r_0=11, 20ms between steps

u= Update flag (Bit 4)

u=1, Update Track register
u=0, No update

In general bit 1 reflects the state of the external DRQ signal while bit 2 indicates lost data due to overrun or underrun conditions. The Type 1 or head positioning instructions use bit 1 and 2 as a reflection of the $\overline{IP}$ and $\overline{TROO}$ inputs respectively.

Bit 3 normally indicates the encounterance of a CRC error in the ID or Data fields except for Read Track and Write Track commands in which the CRC is not checked. Bit 4 indicates that the desired track or sector was not correctly located. Bit 6 reflects the $\overline{WP}$ input on Seek and Write Commands and combines with bit 5 to identify the encountered data address mark on the Read command. Bit 5 also indicates the head engaged status on Seek commands and Write fault or Write commands.

TYPE II

m = Multiple Record flag (Bit 4)

m=0, Single Record
m=1, Multiple Records

b = Block length flag (Bit 3)

b=1, IBM format (128 to 1024 bytes)
b=0, Non-IBM format (16 to 4096 bytes)

a_1a_0 = Data Address Mark (Bits 1-0)

a_1a_0=00, FB (Data Mark)
a_1a_0=01, FA (Data Mark)
a_1a_0=10, F9 (Data Mark)
a_1a_0=11, F8 (Data Mark)

TYPE III

s = Synchronize flag (Bit 0)

$\bar{s}$=0, Synchronize to AM
$\bar{s}$=1, Do not synchronize to AM

TYPE IV

Ii = Interrupt Condition flags (Bits 3-0)

I_0=1, Not Ready to Ready Transition
I_1=1, Ready to Not Ready Transition
I_2=1, Index Pulse
I_3=1, Immediate Interrupt

E=Enable HLD and 10 msec Delay

E=1, Enable HLD, HLT and 10 msec Delay
E=0, Head is assumed Engaged and there is no 10 msec Delay

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1.5 Processor Programming

Some examples of the software control of the Floppy Disk Formatter are shown in the following flow chart. The first example (Figure 1-2) shows the writing of information onto a particular track and sector. The second example (Figure 1-3) shows accessing of information from successive sectors. The third example shows how information may be sought by using Track 00 as a table of contents (Figure 1-4)

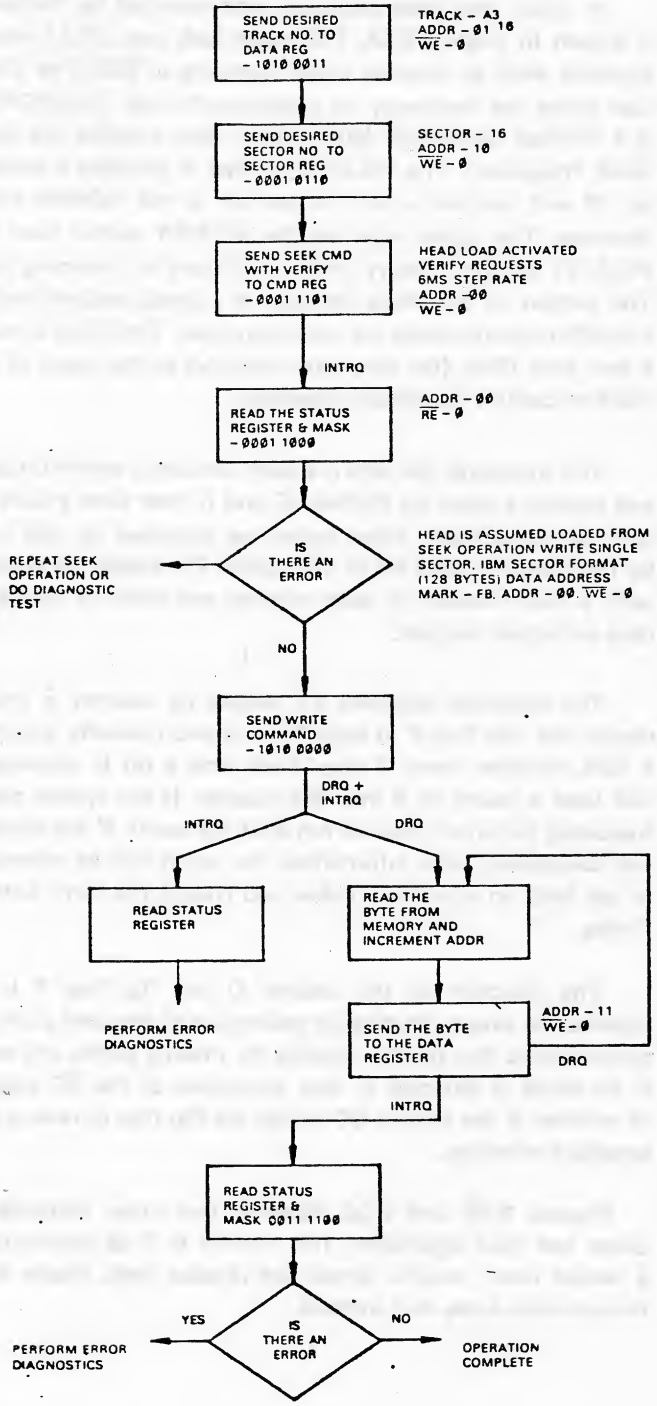

FIGURE 1-2

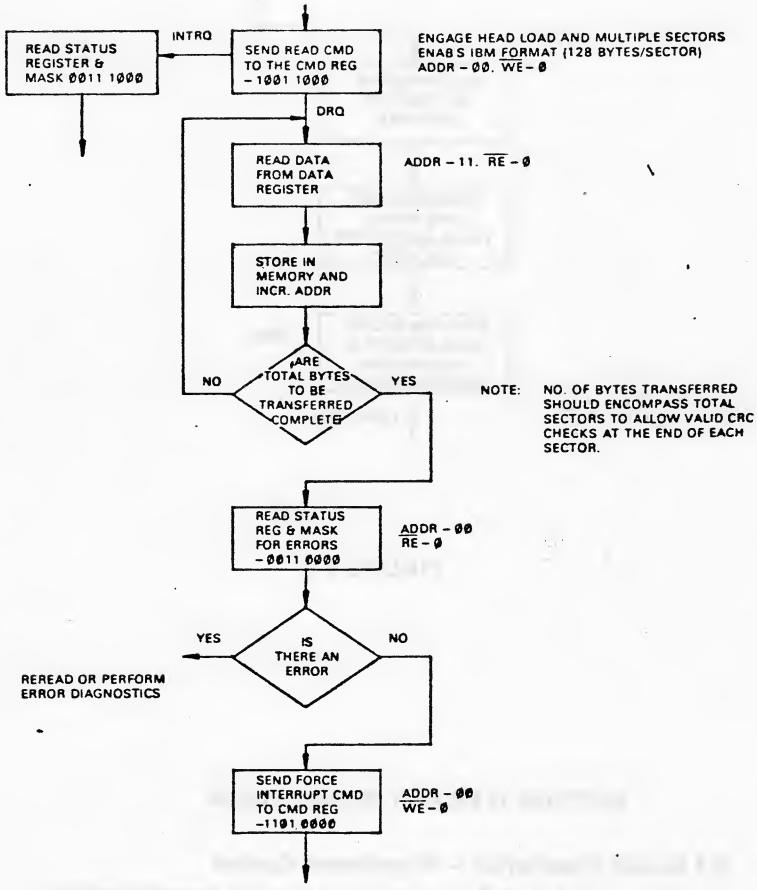

FIGURE 1-3

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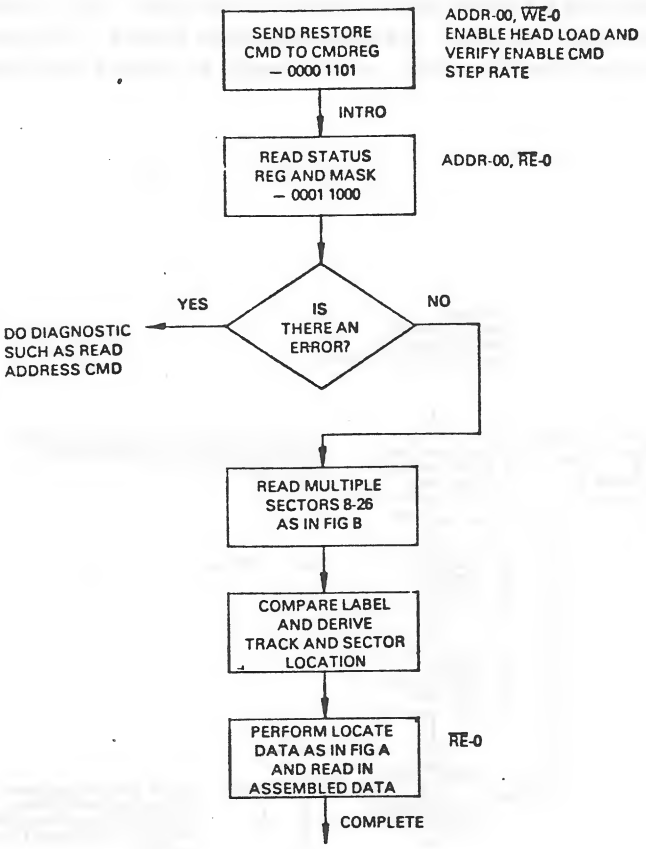

FIGURE 1-4

SECTION II FD1771 INTERFACING

2.1 System Description – Programmed Control

Figures 2-1 to 2-3 demonstrate a possible system configurtion for interfacing a processor to a Floppy Disk drive utilizing the FD1771. This configuration requires the proessor to handle all data transfers which will occur as every 32 μsec.

The chip is selected by addressing it through a pre-assigned address. The lower two bits of this address selects which register is to receive or send data. The Read Enable and Write Enable strobes control the data exchange. The clock may be derived on the board or taken from other processor circuits. Generally the outputs of the FD1771 must be interfaced with drivers and receivers to provide proper matching circuits with the drive. One shots may be necessary to meet the drive's required control signal pulse widths. These circuits must be derived from recommended interfaces specified in Drive manufacturers manuals.

A clock and data separator recommended by Motorola is shown in Fugure 2-3A. This phase lock loop (PLL) circuit operates with an internal clock operating at 8MHZ or thirty two times the frequency of a received bit cell. The MC4024 is a Voltage Controlled Multivibrator that supplies the basic clock frequency. The 74LS161 counter A provides a division by 16 and supplies a carry to one side of the MC4044 phase detector. The other input to the MC4044 comes from the 74LS161 counter E carry which is affected by incoming data. The output of the phase detector is a signal proportional to the differences between the incoming pulses. This is fed through a low pass filter (for long term stability) to the input of the 4024 to control the system frequency.

The incoming raw data is shaped through a schmitt trigger and creates a pulse via flipflops G and H each time a clock or data bit is received. These pulses are stretched to 250 nsec by the one shot J and fed to nand gates. The signals are nanded with a data window or clock window and result in separated data and clock outputs.

The separator windows are formed by counter E which clocks the flip flop F at each 8 count and normally provides a 50% window every 2 μsec. Each time a bit is received it will load a count of 9 into this counter. If the system clock frequency is correct this will not alter the count. If the clock is not concurrent with information the count will be advanced or set back to alter the window and change the carry output timing.

The function of the counter D and flip flop F is to provide the proper phasing for separation of data and clock. It accomplishes this task by looking for missing clocks and data. If no clock is detected in four transitions of the OD output of counter E the output OC causes the flip flop to reverse the sampling windows.

Figures 2-3B and 2-3C illustrate two other methods of clock and data separation. The method in 2-3B incorporates a simple clock counter circuit and phasing logic. Figure 2-3C incorporates a one-shot method.

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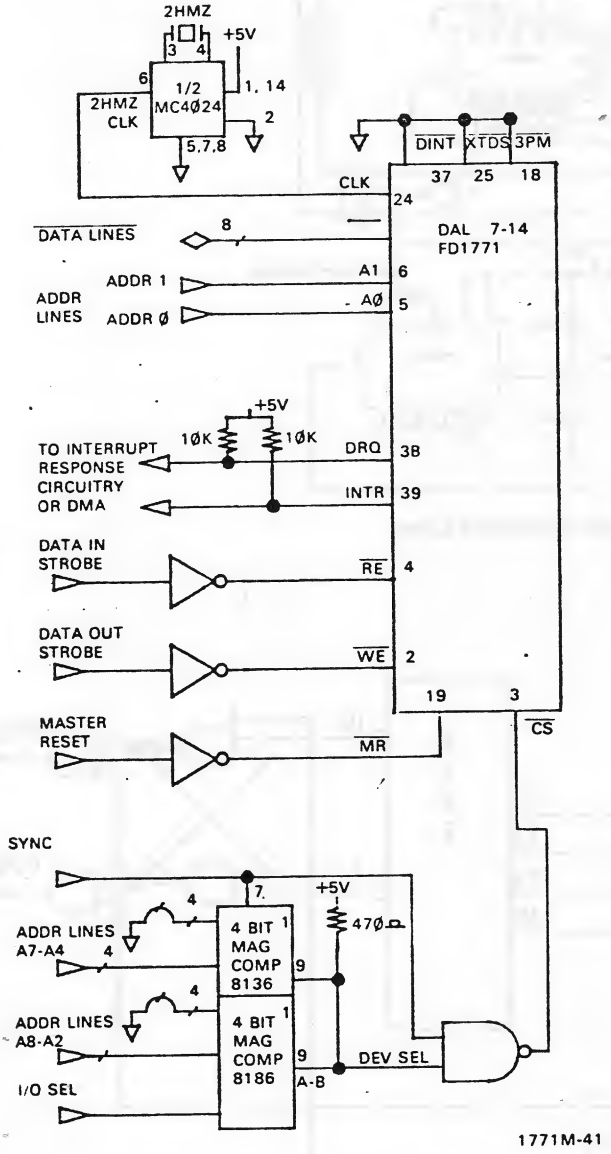

FIGURE 2-1

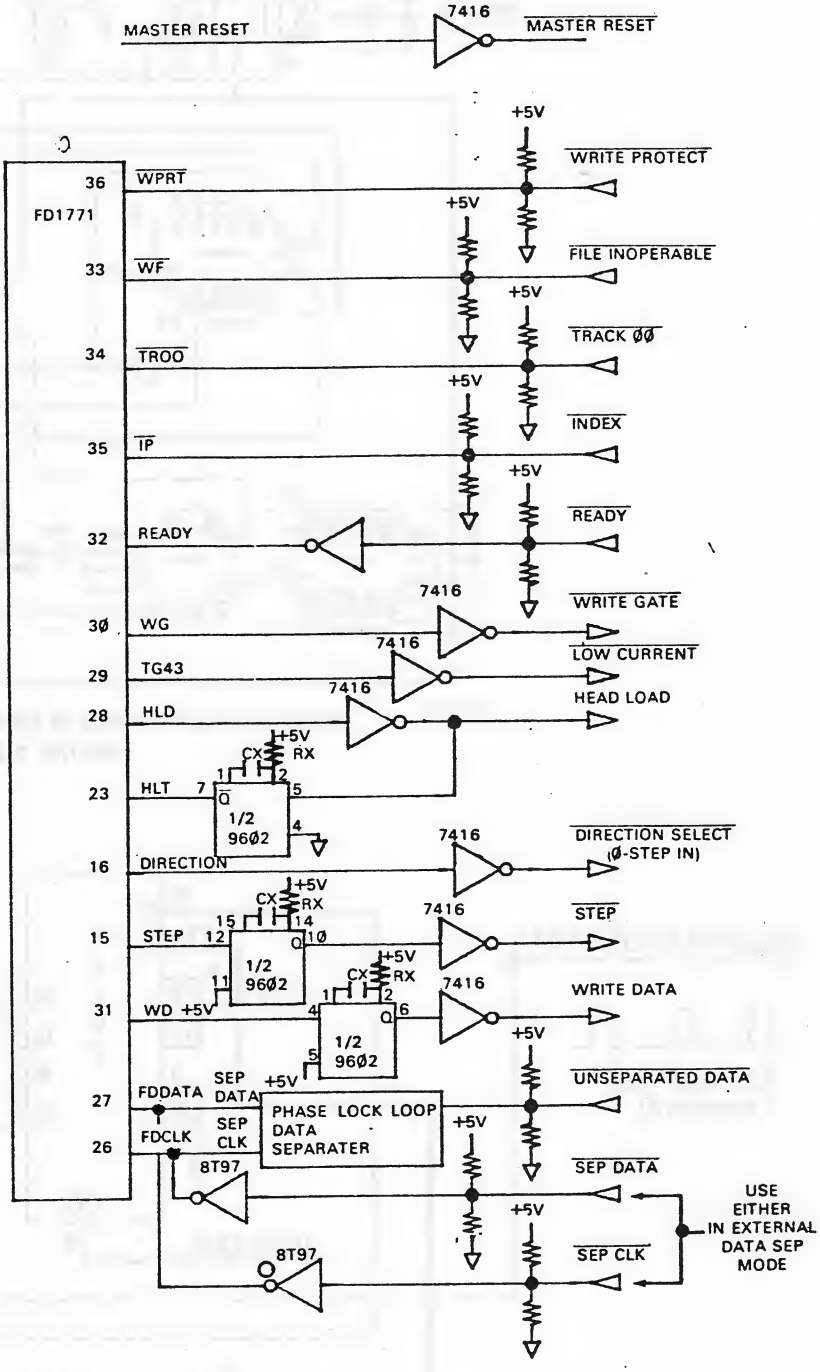

FIGURE 2-2

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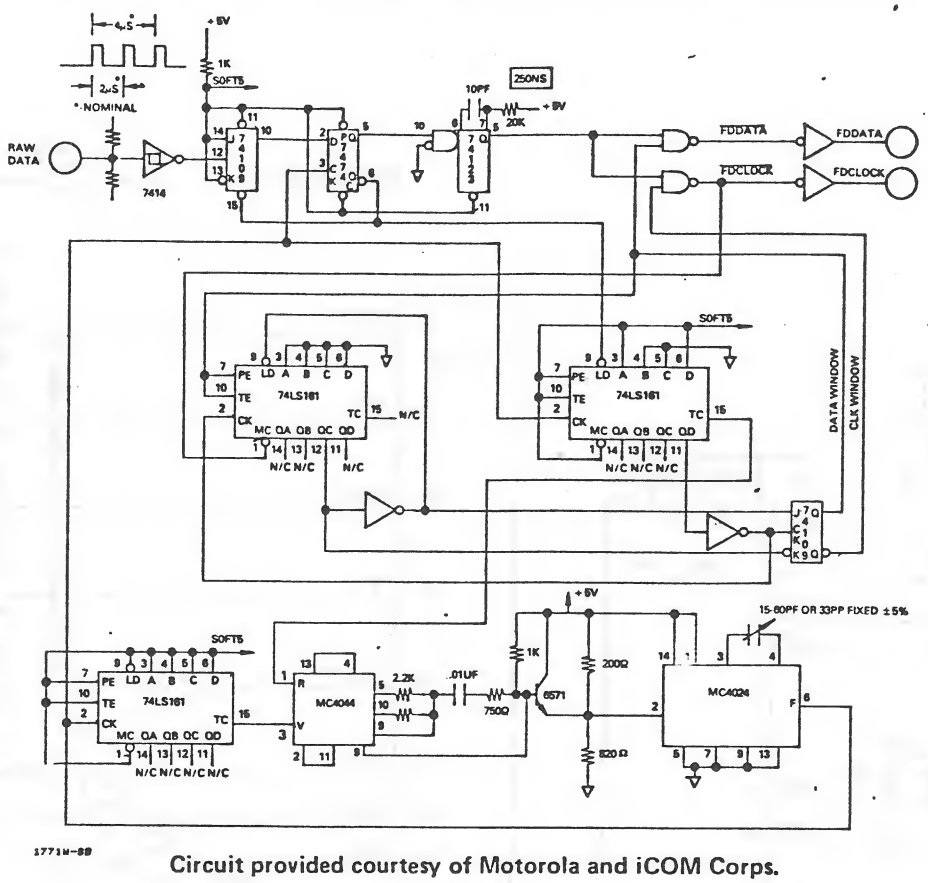
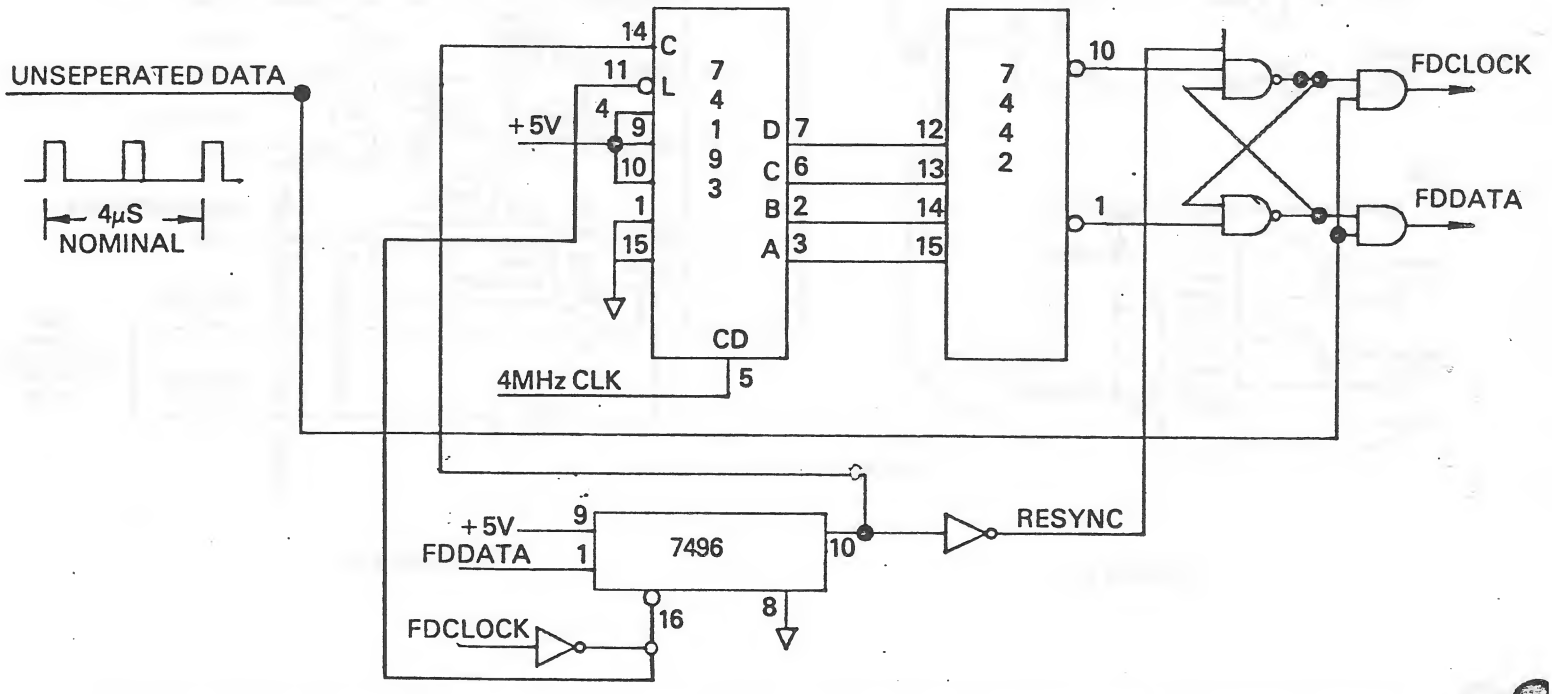


Circuit provided courtesy of Motorola and iCOM Corps.
FIGURE 2-3A



Circuit provided courtesy of Processor Applications Ltd, 2801 E. Valley View, West Covina, Ca. 91792 (213) 965-8865
FIGURE 2-3B

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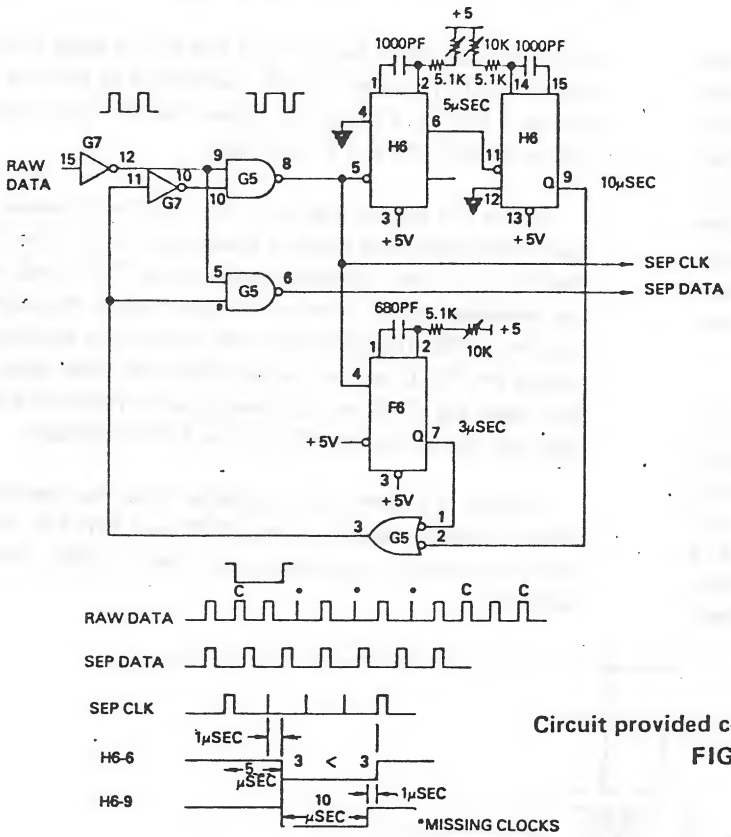

Circuit provided courtesy of Acutest Corp.

FIGURE 2-3C

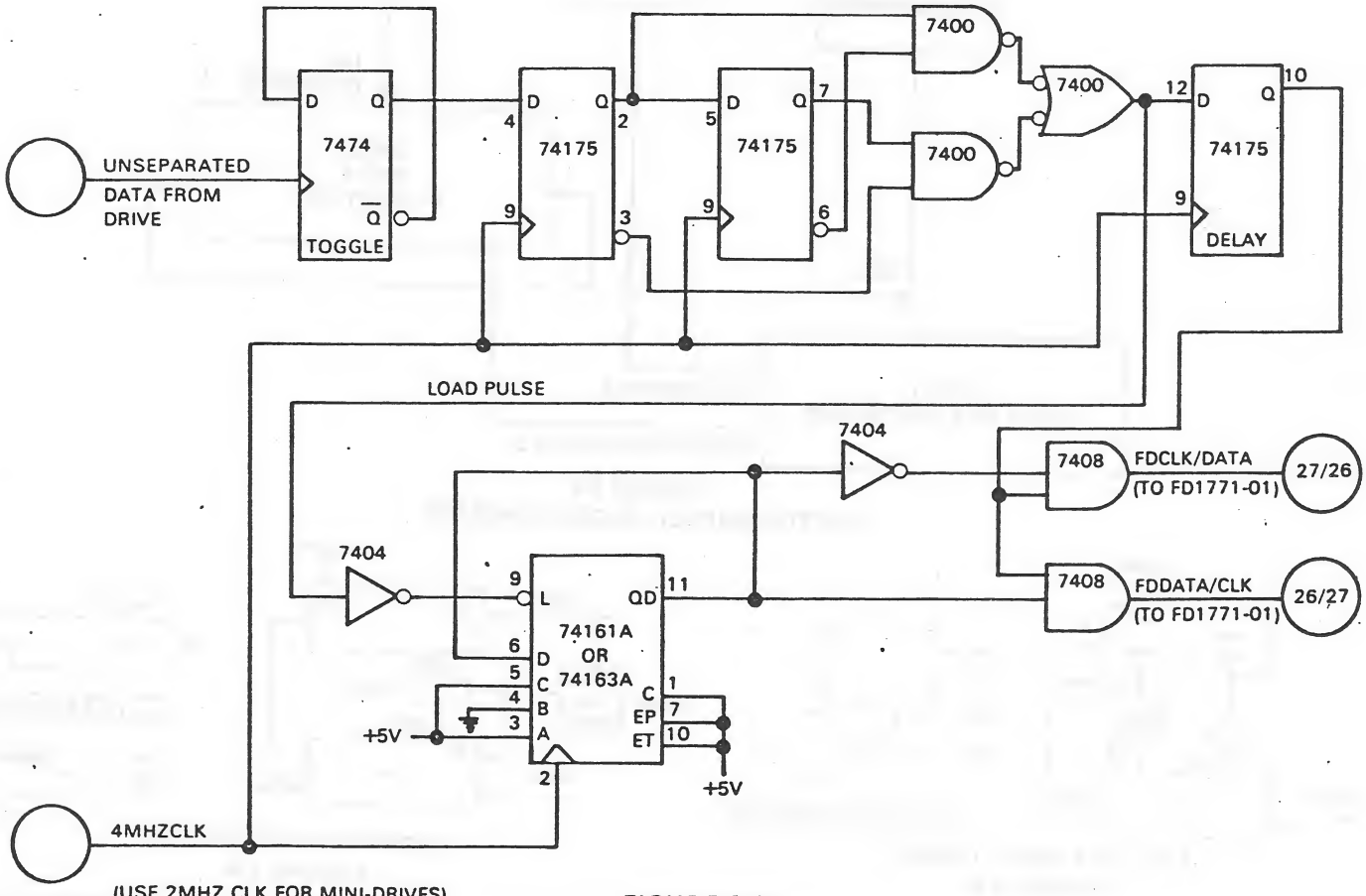

FIGURE 2-3D

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2.2 System Description – Sector buffered

In paragraph 1.1 a program controlled interface was described for the FD1771. This method uses the least number of external IC's but suffers in performance due to the necessity of the processor to service the FD1771 every 32 μsec when transferring data to or from the floppy. It may not be possible for some micro-processors to execute the program loop, within 32 μsec, therefore an alternate method of data transfer must be employed. One such method is to buffer the data transfers in a memory device, thereby requiring the processor to service only interrupt requests.

The block diagram in Figure 2-4 shows the FD1771 interface a FIFO buffer. The buffer consists of 4 FR1502 devices which provide 40 characters by 9 bits each for a total buffer storage of 160 bytes. The select logic provides proper data and command steering for block transfers or program control. The select logic will allow the processor to set a load FIFO mode, transfer a sector of information into the FIFO at processor speed, set the FIFO dump mode and send a write command to the FD1771. The data is then transferred at the rate required by the FD1771. Figure 2-5 shows the interface control and timing in the FIFO to FD interface.

When the floppy disk is to be read the processor sets the load FIFO mode and sends a Read command to the FD1771. The FD1771 then transfers data to the FIFO and interrupts the processor when a sector of information has been loaded into the FIFO. The processor will respond to the interrupt by setting the FIFO to the dump mode and then may read the data from the FIFO at processing speeds. Figure 2-6 shows the logic and timing for the FD1771 to FIFO interface.

Figure 2-7 shows the detailed logic for generating the proper control signals to the FIFO and FD1771. Figure 2-8 shows the proper connection for the FR1502 FIFO buffer memory.

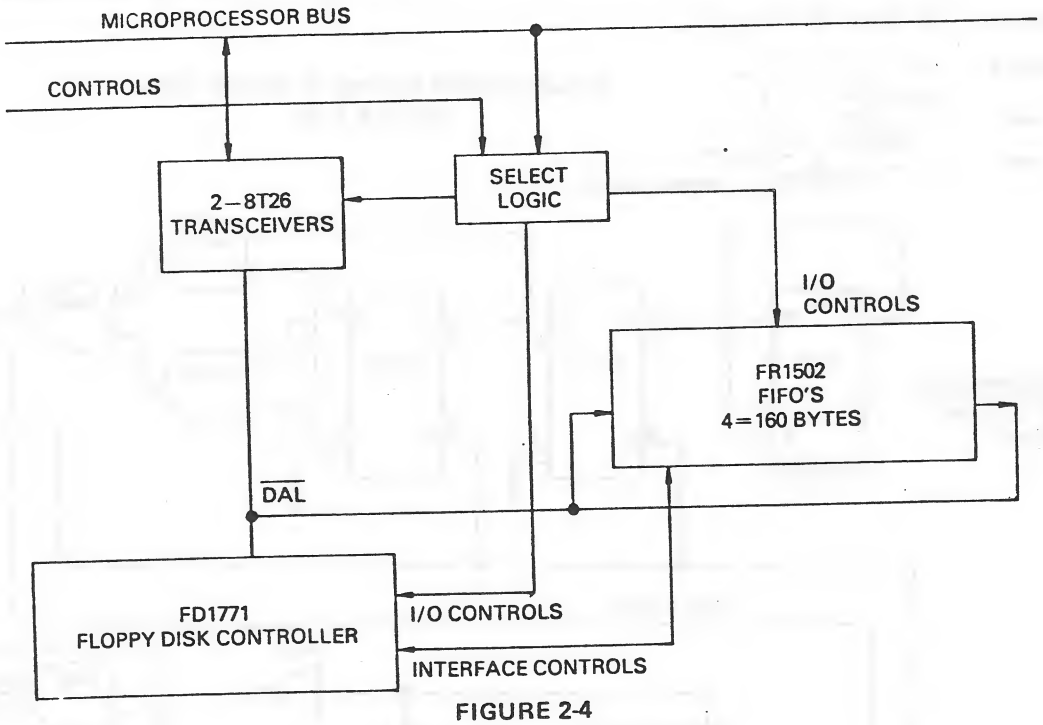
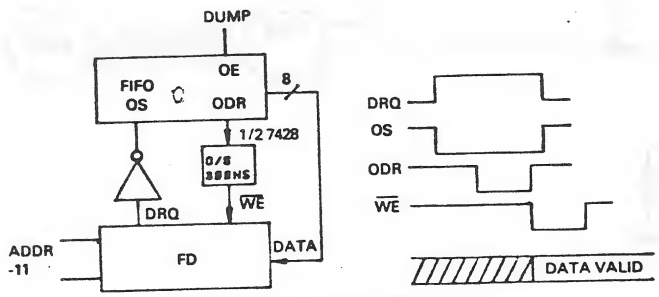
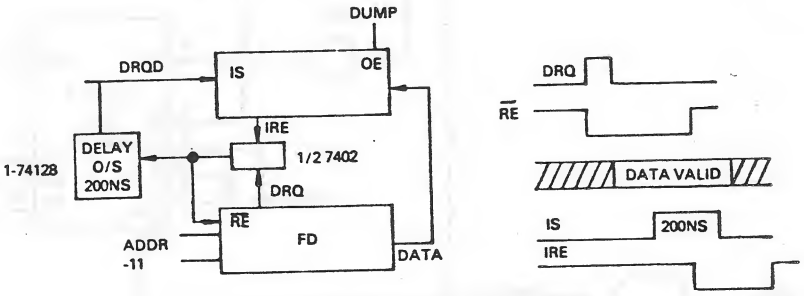


FIGURE 2-4
SECTOR BUFFER BLOCK DIAGRAM



FIFO TO FLOPPY TIMING
FIGURE 2-5



FLOPPY TO FIFO TIMING
FIGURE 2-6

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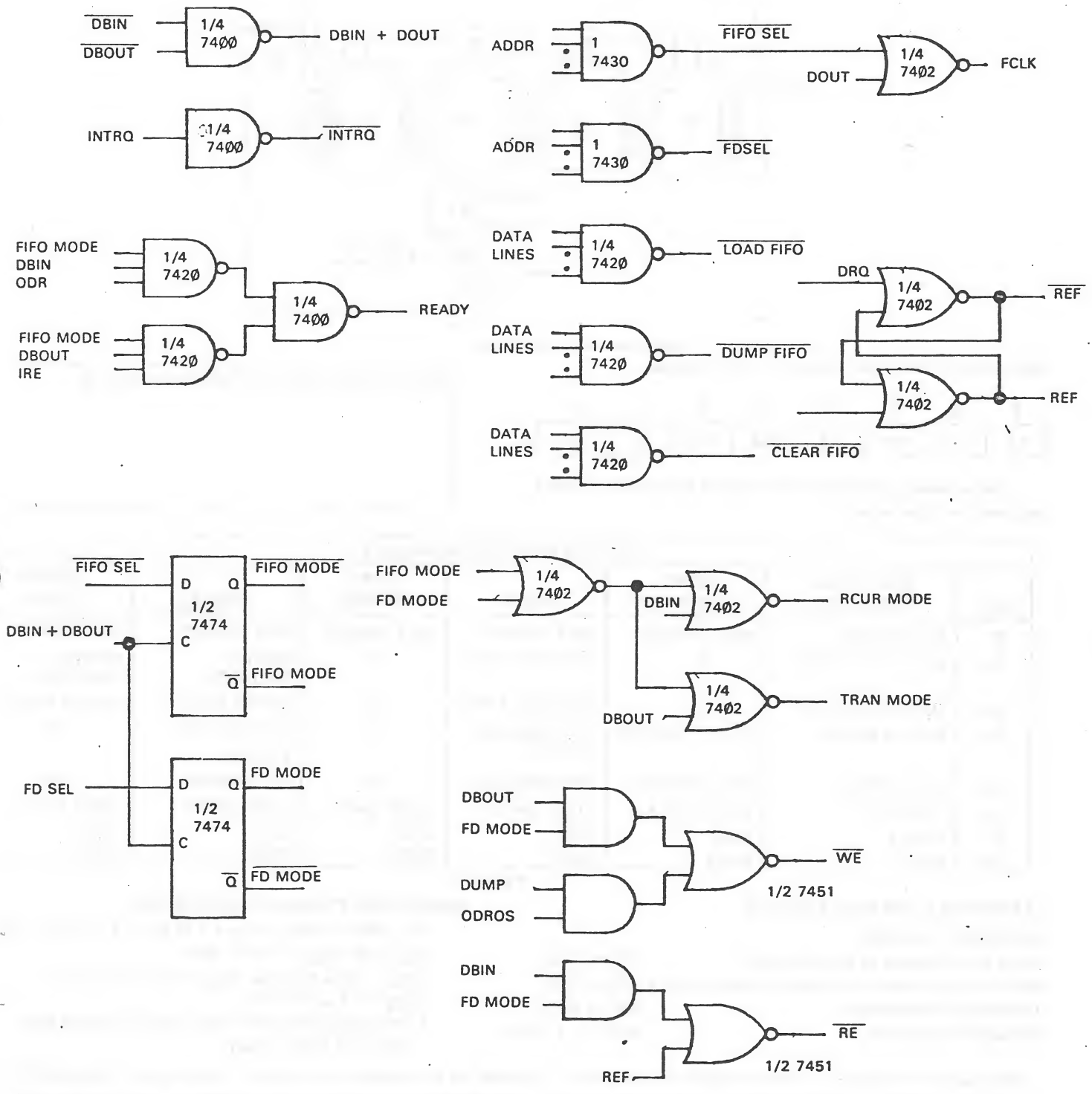

FIGURE 2-7
TIMING CONTROL

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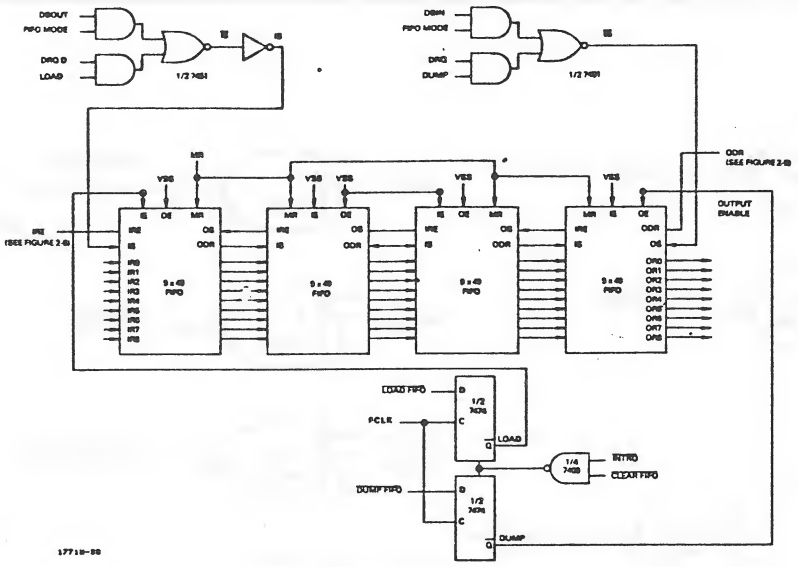

*BIT 8 NOT USED (COULD BE USED FOR PARITY CHECKING IF DESIRED.)

The format of the Status Register is shown below:

7	6	5	4	3	2	1	0
S7	S6	S5	S4	S3	S2	S1	S0

Status varies according to the type of command executed as shown in Table below.

YOUR LOCAL WDC REPRESENTATIVE IS:

STATUS REGISTER SUMMARY						
BIT	ALL TYPE I COMMANDS	READ ADDRESS	READ	READ TRACK	WRITE	WRITE TRACK
S7	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY
S6	WRITE PROTECT	0	RECORD TYPE	0	WRITE PROTECT	WRITE PROTECT
S5	HEAD ENGAGED	0	RECORD TYPE	0	WRITE FAULT	WRITE FAULT
S4	SEEK ERROR	ID NOT FOUND	RECORD NOT FOUND	0	RECORD NOT FOUND	0
S3	CRC ERROR	CRC ERROR	CRC ERROR	0	CRC ERROR	0
S2	TRACK 0	LOST DATA	LOST DATA	LOST DATA	LOST DATA	LOST DATA
S1	INDEX	DRQ	DRQ	DRQ	DRQ	DRQ
S0	BUSY	BUSY	BUSY	BUSY	BUSY	BUSY

TABLE 1

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

V_{DD} With Respect to V_{BB} (Ground)	+20 to -0.3V
Max Voltage to Any Input with Respect to V_{BB}	+20 to -0.3V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C

OPERATING CHARACTERISTICS (DC)

T_A = 0°C to 70°C, V_{DD} = +12.0V ± .6V, V_{BB} = -5.0 ± .5V,
V_{SS} = 0V, V_{CC} = +5V ± .25V
V_{DD} - 10ma Nominal, V_{CC} = 30 ma Nominal,
V_{BB} = 0.4 ua Nominal

* For complete electrical specifications see FD1771 Data Sheet.

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Appendix C -- 6532 PIA Chip Description

1.7.2 R6532

1.7.2.1 Introduction

The R6532 is designed to operate in conjunction with the R6500 Microcomputer System's microprocessor (CPU) family. It is comprised of a 128 x 8 static RAM; two software-controlled, 8-bit bidirectional data ports allowing direct interfacing between the microprocessor unit and peripheral devices; a software programmable interval timer with interrupt, capable of timing in various intervals from 1 to 262,144 clock periods; and a programmable edge-detecting circuit.

- 8-bit bidirectional Data Bus for direct communication with the microprocessor
- 128 x 8 static RAM
- Two 8 bit bidirectional data ports for interface to peripherals
- Two programmable I/O Peripheral Data Direction Registers
- Programmable Interval Timer with Interrupt
- TTL & CMOS compatible peripheral lines
- Peripheral pins with Direct Transistor Drive Capability
- High Impedance Three-State Data Pins
- Programmable edge-sensitive interrupt

1.7.2.2 Pinout Description

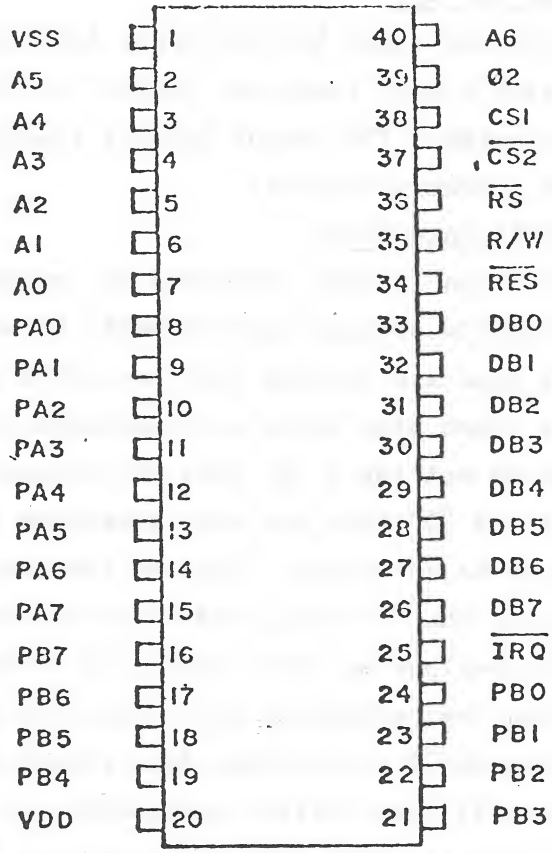
Figure 1.57 is the pinout diagram of the R6532.

1.7.2.2.1 Reset ($\overline{RES}$)

During system initialization a Logic "0" on the $\overline{RES}$ input will cause a zeroing of all four I/O registers. This, in turn, will cause all I/O buses to act as inputs, thus protecting external components from possible damage and erroneous data while the system is being configured under software control. The Data Bus Buffers are put into an OFF-STATE during Reset. Interrupt capability is disabled with the $\overline{RES}$ signal. The $\overline{RES}$ signal must be held low for at least one clock period when reset is required.

1.7.2.2.2 Input Clock

The input clock is a system Phase 2 clock which can be either a low-level clock ($V_{IL} < 0.4$, $V_{IH} > 2.4$) or a high-level clock ($V_{IL} < 0.2$, $V_{IH} = Vcc \begin{smallmatrix}+0.3\\-0.2\end{smallmatrix}$).



R6532 Pinout Designation

FIGURE 1.57

1.7.2.2.3 Read/Write (R/W)

The R/W signal is supplied by the microprocessor array and is used to control the transfer of data to and from the microprocessor array and the R6532. A high on the R/W pin allows the processor to read (with proper addressing) the data supplied by the R6532. A low on the R/W pin allows a write (with proper addressing) to the R6532.

1.7.2.2.4 Interrupt Request (IRQ)

The $\overline{IRQ}$ pin is an interrupt pin from the interrupt control logic. The pin will be normally high, with a low indicating an interrupt from the R6532. An external pull-up device is required. The $\overline{IRQ}$ pin may be activated by a transition on PA7 or timeout of the interval timer.

1.7.2.2.5 Data Bus (D0-D7)

The R6532 has eight bidirectional data pins (D0-D7). These pins connect to the system's data lines and permit transfer of data to and from the microprocessor array. The output buffers remain in the "off" state except when a Read operation occurs.

1.7.2.2.6 Peripheral Data Ports

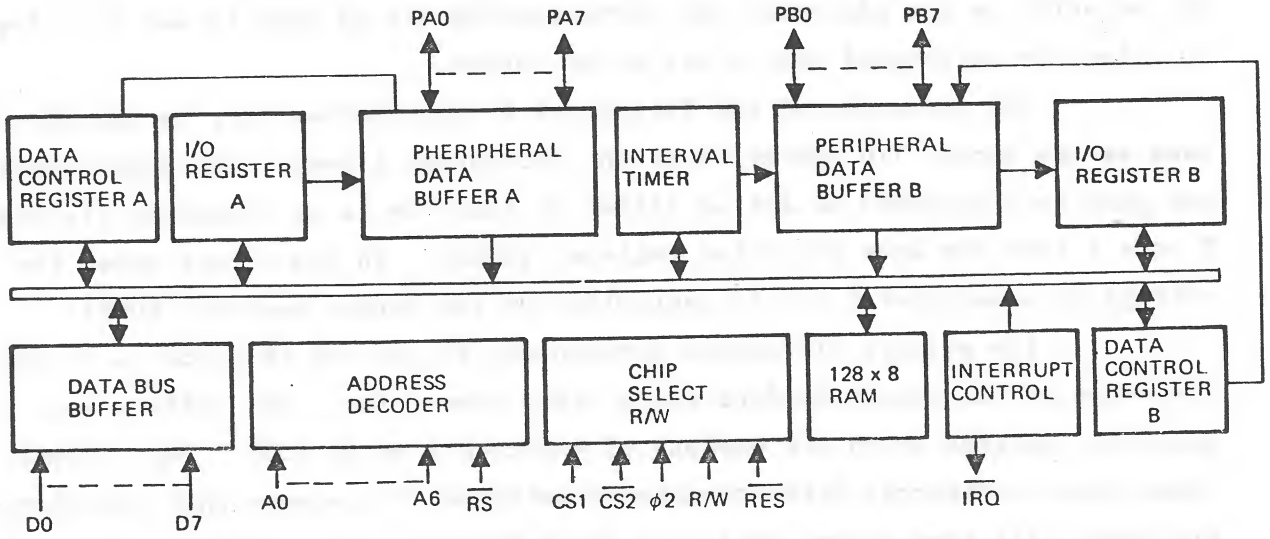
The R6532 has 16 pins available for peripheral I/O operations. Each pin is individually software-programmable to act as either an input or an output. The 16 pins are divided into two 8-bit ports, PA0-PA7 and PB0-PB7. PB7 also has other uses which are discussed elsewhere. The pins are set up as an input by writing a "0" into the corresponding bit of the data direction register. A "1" into the data direction register will cause its corresponding bit to be an output. When in the input mode, the peripheral output buffers are in the "1" state and a pull-up device acts as less than one TTL load to the peripheral data lines. On a Read operation, the microprocessor unit reads the peripheral pin. When the peripheral device gets information from the R6532 it receives data stored in the data register. The microprocessor will read correct information if the peripheral lines are greater than 2.0 volts for a "1" and less than 0.8 volt for a "0" as the peripheral pins are all TTL compatible. Pins PB0-PB7 are also capable of sourcing 3 ma at 1.5V, thus making them capable of Darlington drive.

1.7.2.2.7 Address Lines (A0-A6)

There are 7 address pins. In addition to these 7, there is the $\overline{\text{RAM SELECT}}$ pin. The above pins, A0-A6 and $\overline{\text{RAM SELECT}}$, are always used as addressing pins. There are two additional pins which are used as CHIP SELECTs. They are pins CS1 and $\overline{\text{CS2}}$.

1.7.2.3 Internal Organization

A block diagram of the internal architecture is presented in Figure 1.58. The R6532 is divided into four basic sections, RAM, I/O, Timer, and Interrupt Control. The RAM interfaces directly with the microprocessor through the system data bus and address lines. The I/O section consists of two 8-bit halves, each of which contains a Data Direction Register (DDR) and an I/O Register.



R6532 Internal Architecture

FIGURE 1.58

1.7.2.3.1 RAM - 128 Bytes (1024 Bits)

The 128 x 8 Read/Write memory acts as a conventional static RAM. Data can be written into the RAM from the microprocessor by selecting the chip (CS1 = 1, $\overline{CS2}$ = Ø) and by setting $\overline{RS}$ to a logic Ø (0.4V). Address lines A0 through A6 are then used to select the desired byte of storage.

1.7.2.3.2 Internal Peripheral Registers

The Peripheral A I/O port consists of eight lines which can be individually programmed to act as either an input or an output. A logic 0 in a bit of the Data Direction Register (DDRA) causes the corresponding line of the PA port to act as an input. A logic 1 causes the corresponding PA line to act as an output. The voltage on any line programmed to be an output is determined by the corresponding bit in the Output Register (ORA).

Data are read directly from the PA pins during any read operation. For any output pin, the data transferred into the processor will be the same as those contained in the Output Register if the voltage on the pin is allowed to go to 2.4V for a logic one. Note that for input lines, the processor can

write into the corresponding bit of the Output Register. This will not affect the polarity on the pin until the corresponding bit of DDRA is set to a logic 1 to allow the peripheral pin to act as an output.

The operation of the Peripheral B Input/Output port is exactly the same as the normal I/O operation of the Peripheral A port. The eight lines can each be programmed to act as either an input or as an output by placing a 0 or a 1 into the Data Direction register (DDRB). In the output mode, the voltage on a peripheral pin is controlled by the Output Register (ORB).

The primary difference between the PA and the PB ports is in the operation of the output buffers which drive these pins. The buffers are push-pull devices which are capable of sourcing 3 ma at 1.5V. This allows these pins to directly drive transistor switches. To ensure that the microprocessor will read proper data on a "Read PB" operation, sufficient logic is provided in the chip to allow the microprocessor to read the Output Register instead of reading the peripheral pin as on the PA port.

1.7.2.3.3 Edge-Detecting Interrupt

In addition to acting as a peripheral I/O line, the PA7 line can serve as an edge-detecting input. In this mode, an active transition will set the internal interrupt flag (bit 6 of the Interrupt Flag register). Setting the interrupt flag will cause IRQ output to go low if the PA7 interrupt has been enabled.

Control of the PA7 edge-detecting mode is accomplished by writing to one of four addresses. In this operation, A0 controls the polarity of the active transition and A1 acts to enable to disable interrupting of the processor. The data placed on the Data Bus during this operation are discarded and have no effect on the control of PA7.

Setting of the PA7 interrupt flag will occur on an active transition even if the pin is being used as a normal input or as a peripheral control output. The flag will also be set by an active transition if interrupting from PA7 is disabled. The reset signal ($\overline{RES}$) will disable the PA7 interrupt and will set the active transition to negative (high to low). During the system initialization routine, it is possible to set the interrupt flag by a negative transition. It may also be set by changing the polarity of the active interrupt. It is therefore recommended that the interrupt flag be cleared before enabling interrupting from PA7.

Clearing of the PA7 Interrupt Flag occurs when the microprocessor reads the Interrupt Flag Register.

1.7.2.3.4 Interval Timer

The Timer section (Figure 1.59) of the R6532 contains a preliminary divide-down register, a programmable 8-bit register, and interrupt logic.

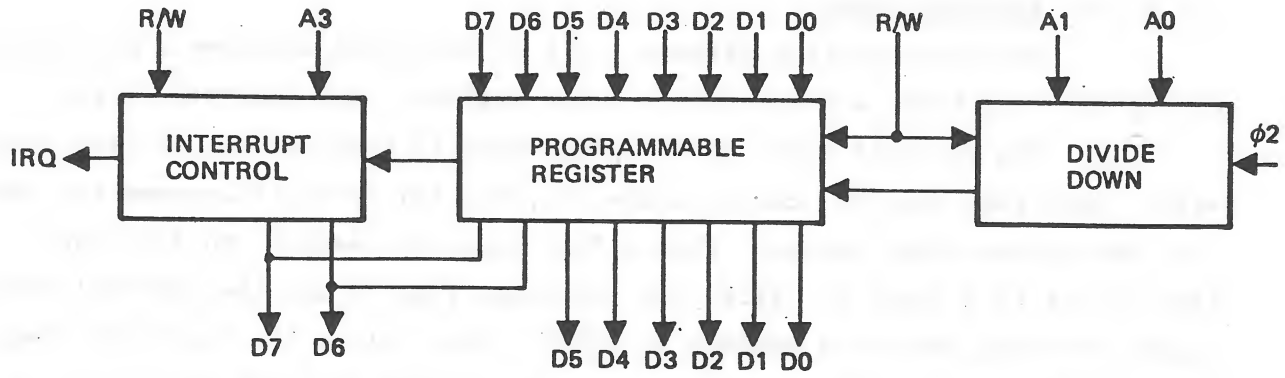
The Interval Timer can be programmed to count up to 255 time intervals. Each time interval can be either 1T, 8T, 64T or 1024T increments, where T is the system clock period. When a full count is reached, an interrupt flag is set to a logic 1. After the interrupt flag is set the internal clock begins counting down to a maximum of -255T. Thus, after the interrupt flag is set, a Read of the Timer will tell how long since the flag was set up to a maximum of 255T.

The 8-bit system Data Bus is used to transfer data to and from the Interval Timer. If a count of 52 time intervals were to be counted, the pattern 0 0 1 1 0 1 0 0 would be put on the Data Bus and written into the Interval Time register.

At the same time that data are being written to the Interval Timer, the counting intervals of 1, 8, 64, 1024T are decoded from address lines A0 and A1. During a Read or Write operation address line A3 controls the interrupt capability of PB7, i.e. $A_3 = 1$ enables $\overline{IRQ}$, $A_3 = 0$ disables $\overline{IRQ}$. When the the timer is read prior to the interrupt flag being set, the number of time intervals remaining will be read, i.e., 51, 50, 49, etc.

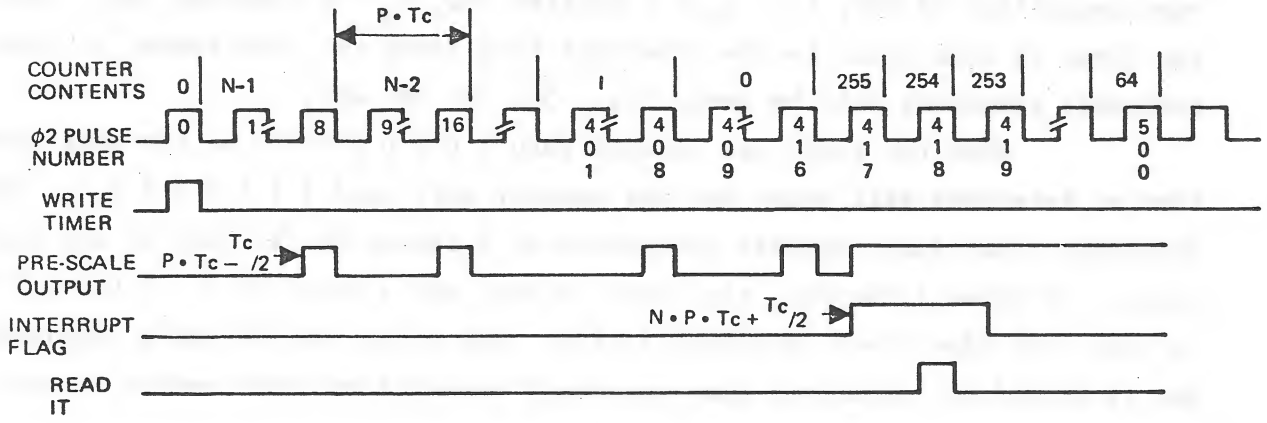
When the timer has counted thru 0 0 0 0 0 0 0 0 on the next count time an interrupt will occur and the counter will read 1 1 1 1 1 1 1 1. After interrupt, the timer register decrements at a divide by "1" rate of the system clock. If after interrupt, the timer is read and a value of 1 1 1 0 0 1 0 0 is read, the time since interrupt is 27T. The value read is two's complement, but it should be remembered that interrupt occurred on count number -1 and we must, therefore, subtract 1:

Value read = 1 1 1 0 0 1 0 0
Complement = 0 0 0 1 1 0 1 1
ADD 1 = 0 0 0 1 1 1 0 0 = 28 Equals two's complement of register
SUB 1 = 0 0 0 1 1 0 1 1 = 27



Basic Elements of Interval Timer

FIGURE 1.59



ASSUME 52 LOADED INTO TIMER WITH A DIVIDE BY 8.
THE COUNTER CONTENTS AND THE CLOCK PULSE NUMBERS WILL COINCIDE.

Interval Timer Example

FIGURE 1.60

Thus, to arrive at the total elapsed time, one merely carries out a two's complement add to the original time written into the timer. Again, time is to be assumed to be written as 0 0 1 1 0 1 0 0 (=52). With a divide by 8, total time to interrupt is (52 x 8) + 1 = 417T. Total elapsed time would be 417T + 27T = 444T, assuming the value read after interrupt was 1 1 1 0 0 1 0 0.

After the interrupt, whenever the timer is written or read the interrupt is reset. However, the reading of the timer at the same time the interrupt occurs will not reset the interrupt flag. When the interrupt flags are read (DB7 for the timer, DB6 for edge detect) data bus lines D0-D5 go to zero.

When reading the timer after an interrupt, A3 should be low to disable the $\overline{IRQ}$ pin. This is done to avoid future interrupts until after another Write timer operation.

RAM ADDRESSING

$\overline{RS}$ = 0
RW = 1 to read, 0 to write
AØ-A6 select RAM address

I/O ADDRESSING

$\overline{RS}$ = 1 A2 = 0
RW = 1 to read, 0 to write

	A1	AØ
PA data	0	0
PA data direction	0	1
PB data	1	0
PB data direction	1	1

WRITE EDGE-DETECTION CONTROL

$\overline{RS}$, A2 = 1 R/W, A4 = 0

A1 = 1, enable interrupt from PA7
A1 = 0, disable interrupt from PA7
A0 = 1, positive edge detect
A0 = 0, negative edge detect

READ AND CLEAR INTERRUPT FLAG

$\overline{RS}$, R/W, A2, AØ = 1

Bit 7 = Timer Flag
Bit 6 = PA7 Flag

WRITE COUNT TO INTERVAL TIMER

$\overline{RS}$, A4, A2 = 1 R/W = 0

	A1	AØ
÷ 1	0	0
÷ 8	0	1
÷ 64	1	0
÷ 1024	1	1

A3 = 1 enable timer interrupt
A3 = 0 disable timer interrupt

NOTE: For all operations CS1 = 1, $\overline{CS2}$ = 0.

Addressing Decode for R6532
FIGURE 1.61

Appendix D -- 6507 Microcomputer Description

The R6502 provides a full 16-bit address bus, 8-bit bidirectional data bus, and two interrupts. In addition, the R6502 provides a sync signal which indicates those cycles in which the processor is fetching an operation code from program memory.

1.2.2 The R6503 through R6507 and R6513 through R6515

Eight 28-pin versions of the processor are available. These eight differ in the number of address lines and the clock generation methods required, the number of interrupts provided. Having all three options available allows the designer to tailor his processor to his particular application.

The R6504 and R6507 provide a total of 13 address pins and can, therefore, address a full 8K bytes in its memory space. The R6504 provides only one interrupt request input, $\overline{IRQ}$; the R6507 provides a RDY input instead of $\overline{IRQ}$. The non-maskable interrupt ($\overline{NMI}$) is not included in the pinouts of this device.

The R6503 and R6505 provide one less address line. In the R6503 the missing address line is replaced with a second interrupt input, $\overline{NMI}$ and in the R6505 it is replaced by the RDY signal. All other functions on these processors are the same. The details of each of the pins are discussed in the following sections.

The operation of the various busses, control signals, etc. is exactly the same on all R650X products, with all processors obeying the system specifications discussed in Section 1.3 of this manual.

The R6513 is the slave (clocks driven in) version of the R6503, the R6514 is the slave version of the R6504, and the R6515 is the slave version of the R6505.

1.3 R6500 SYSTEM CONCEPTS

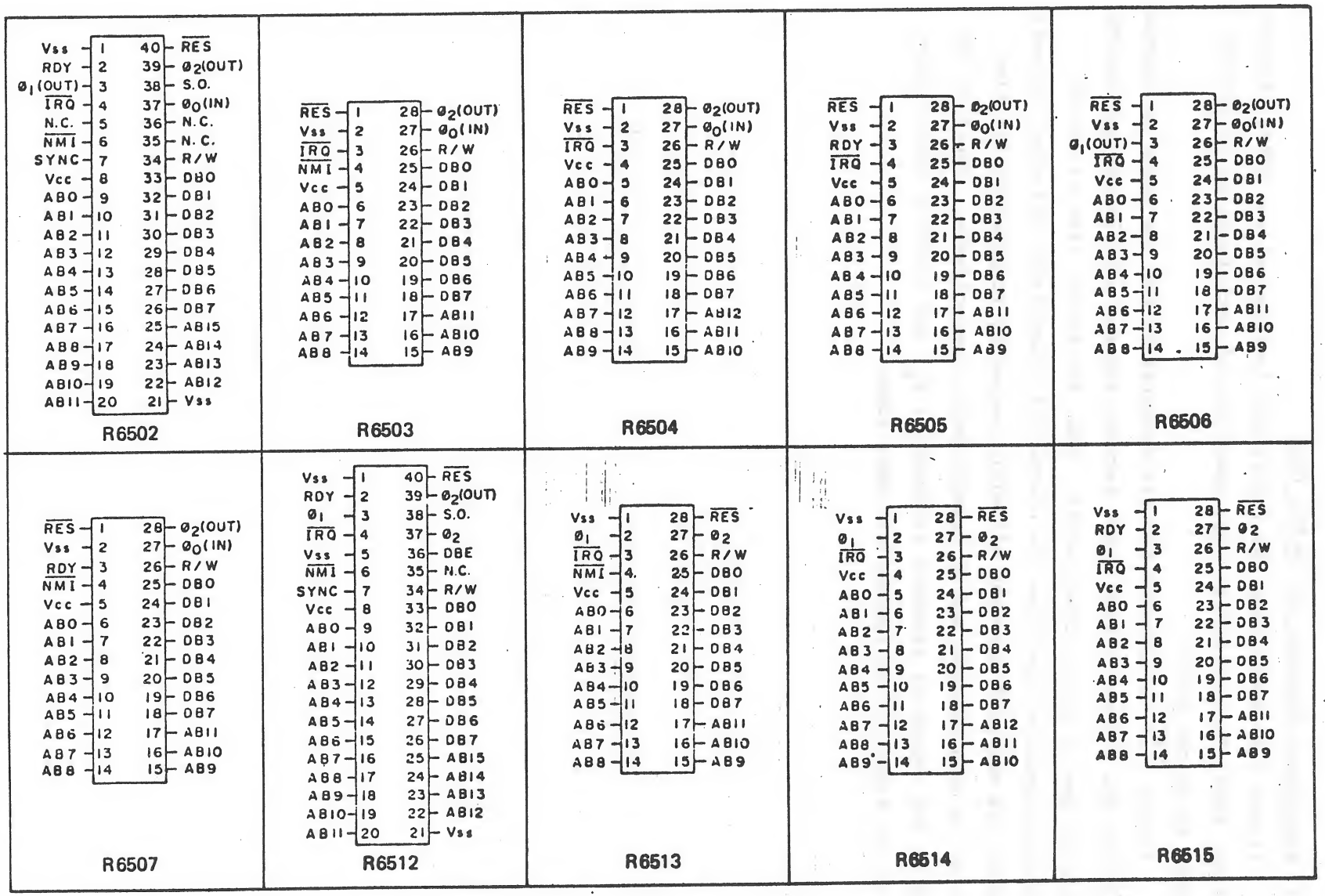
1.3.1 Bus Structure

The R6500 microcomputer system is organized around two primary busses. Each bus consists of a set of parallel paths which can be used to transfer binary information between the devices in a system. The first bus, known as the ADDRESS BUS, is used to transfer the address generated by the processor

1.4.4 Functional Features of 28-Pin CPUs

Figure 1.17 summarizes the functional features of the R6503 through R6507 and R6513 through R6515. The operation of each function is exactly the same as on the R6502.

Figure 1.12 illustrates the pin designation for the eight processors, indicating the tradeoffs that exist between control signals and addressing capability due to pinout constraints. Like the R6502, five of the 28 pin microprocessors also have the on-the-chip oscillator and clock drivers. Figures 1.18 and 1.19 show the circuitry necessary to generate the time base in the crystal mode and RC network mode, respectively. Specific details on the values of feedback resistance, R_F, and feedback capacitance, C_F, can be found in the appropriate data sheet.



CPU Pinout Designations

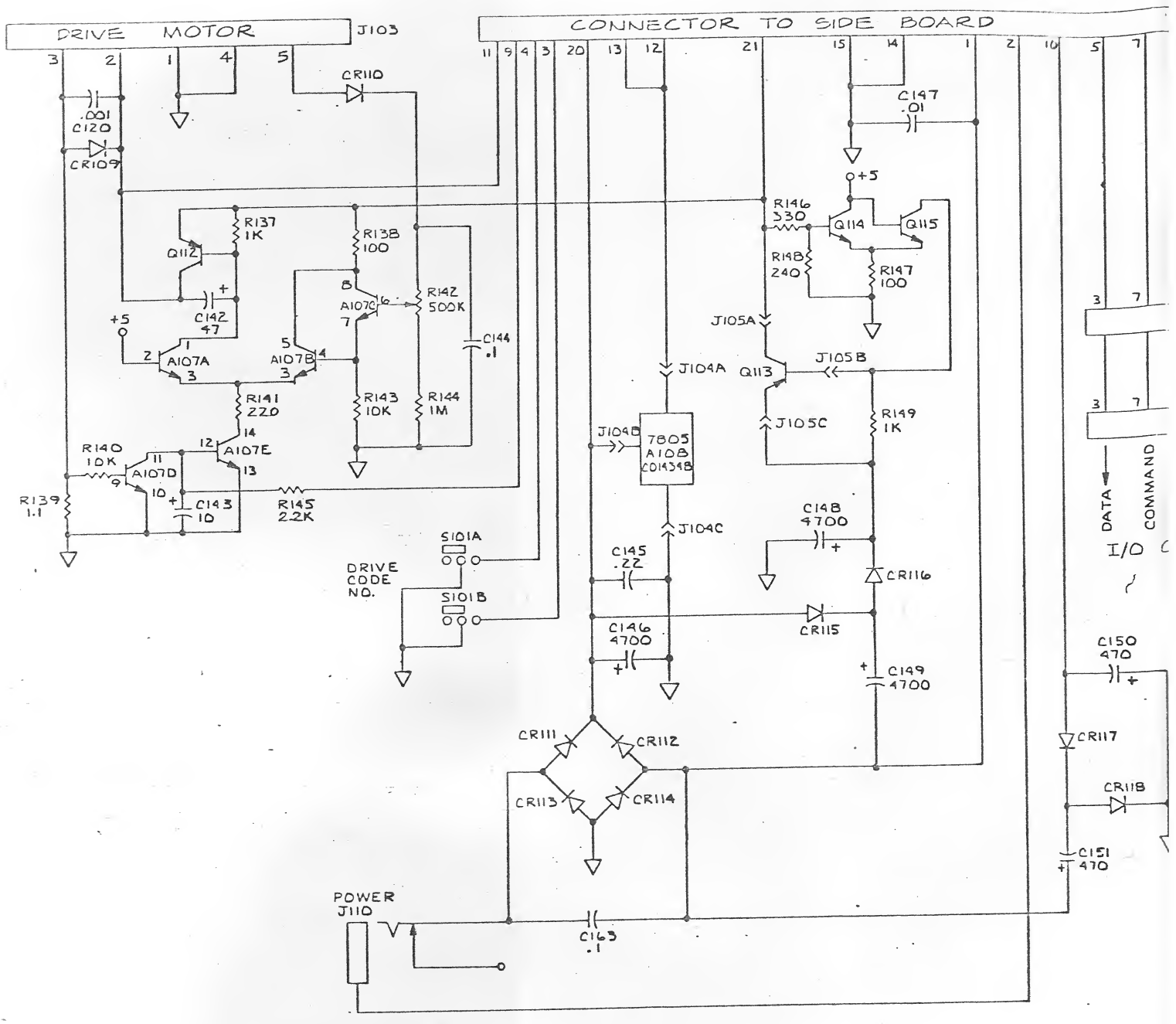
FIGURE 1.11

Features	R6503, R6513	R6504, R6514	R6505, R6515	R6506	R6507
Addressing Capability	4096 Bytes (AB00 - AB11)	8192 Bytes (AB00 - AB12)	4096 Bytes (AB00 - AB11)	4096 Bytes (AB00 - AB11)	8192 Bytes (AB00 - AB12)
Interrupt Request Capability	$\overline{IRQ}$, $\overline{NMI}$	$\overline{IRQ}$	$\overline{IRQ}$	$\overline{IRQ}$	--
"Ready" Signal	--	--	RDY	--	RDY
*Timing Signals Required	Single Phase TTL Level $\emptyset_0$ (IN), or Crystal or RC	Single Phase TTL Level $\emptyset_0$ (IN), or Crystal or RC	Single Phase TTL Level $\emptyset_0$ (IN), or Crystal or RC	Single Phase TTL Level $\emptyset_0$ (IN) or Crystal or RC	Single Phase TTL Level $\emptyset_0$ (IN), or Crystal or RC
Other Control Signals	$\overline{RES}$, R/W	$\overline{RES}$, R/W	$\overline{RES}$, RW	$\emptyset_1$ (OUT), $\overline{RES}$, R/W	$\overline{RES}$, R/W

*6513, 6514 and 6515 are slave microprocessors requiring external $\emptyset_1$ and $\emptyset_2$ clock inputs

Functional Features of 28-Pin CPUs

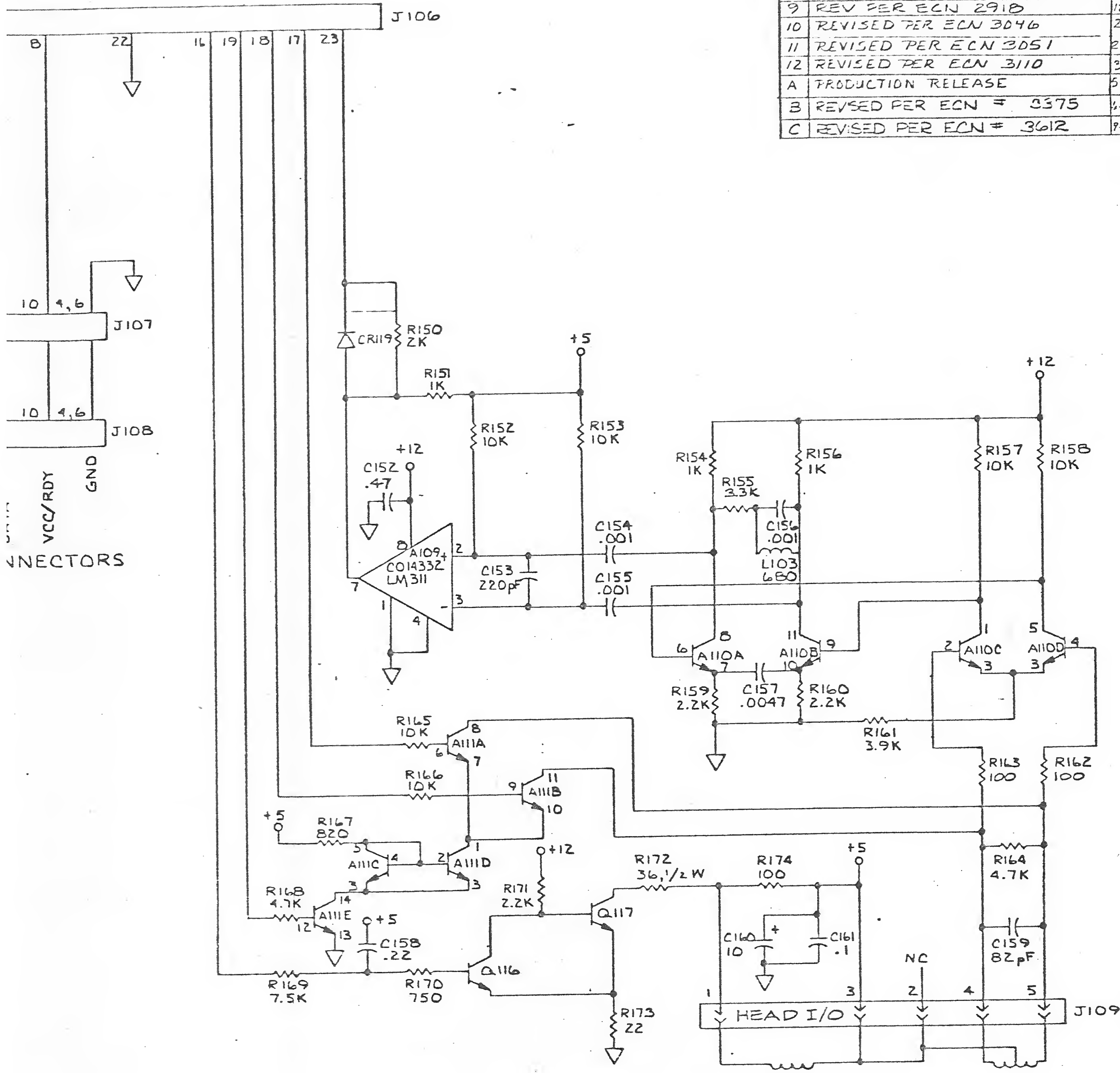
FIGURE 1.17



NOTE:

1. UNLESS OTHERWISE SPECIFIED
   A) ALL CAPACITORS ARE IN μF
   B) ALL RESISTORS ARE IN OHMS, 1/4 W, 5%

SYM	REVISIONS DESCRIPTION	DATE	APPROVED
1	PROTO RELEASE		
2	UPDATE DWG		
3	UPDATE DWG		
4	REV PER ECN 2786	7/12/7	
5	REVISED PER ECN 2827	10-19-75	
6	REVISED PER ECN 2884	11-19-77	
7	REVISED PER ECN 2903	11-23-77	
8	REVISED PER ECN 2912	12/1/77	
9	REV PER ECN 2918	12-1-77	
10	REVISED PER ECN 3046	2-22-80	
11	REVISED PER ECN 3051	2-28-80	
12	REVISED PER ECN 3110	3-18-80	
A	PRODUCTION RELEASE	5-16-80	
B	REVISED PER ECN # 3375	8-12-80	
C	REVISED PER ECN # 3612	9-22-80	



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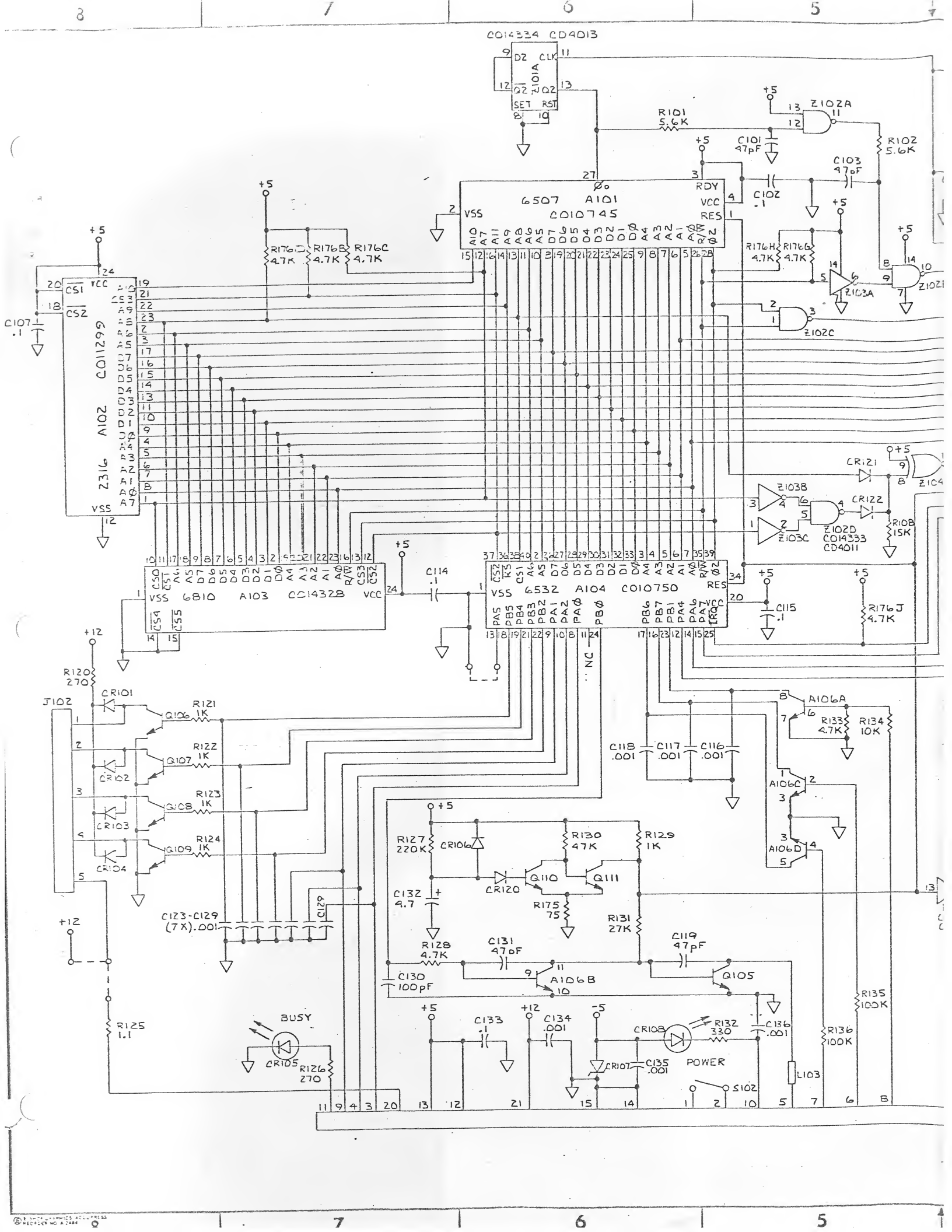
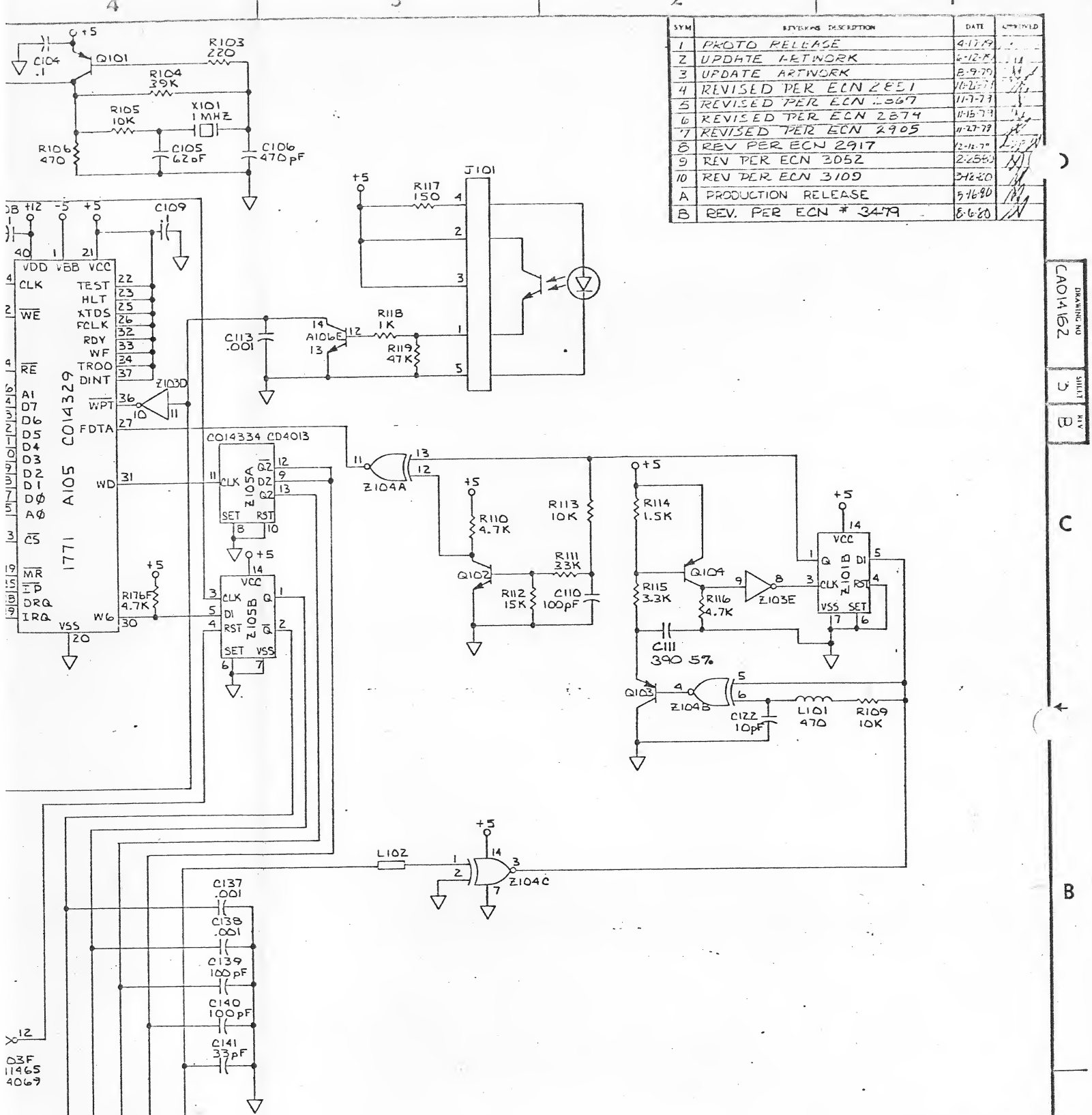

8
7
6
5
CO14334 CD4013
Z101A
Z101B
Z102
R101 5.6K
Z102A
R102 5.6K
C101 47pF
C103 47pF
C102 .1
6507 A101 CO10745
RDY
VCC
RES
VSS
R176D 4.7K
R176B 4.7K
R176C 4.7K
R176H 4.7K
R176G 4.7K
Z103A
Z102B
Z102C
C107 .1
2316 A102 CO11299
VCC
VSS
Z103B
Z103C
Z102D
CD14333
CD4011
CR121
CR122
R108 15K
6810 A103 CO14328
C114 .1
6532 A104 CO10750
C115 .1
R176J 4.7K
R120 270
J102
CR101
Q106
R121 1K
CR102
Q107
R122 1K
CR103
Q108
R123 1K
CR104
Q109
R124 1K
C123-C129 (7X).001
C129
A106A
A106B
A106C
A106D
R133 4.7K
R134 10K
C118 .001
C117 .001
C116 .001
R127 220K
CR106
R130 47K
R129 1K
CR120
Q110
Q111
C132 4.7
R175 75
R131 27K
C119 47pF
R128 4.7K
C131 47pF
C130 100pF
Q105
R135 100K
R136 100K
R125 1.1
BUSY
CR105
R126 270
C133 .1
C134 .001
CR108
R132 330
C136 .001
CR107
C135 .001
POWER
L103
S102
NC

SYM	REVISIONS DESCRIPTION	DATE	APPROVED
1	PROTO RELEASE	4-17-79	
2	UPDATE ARTWORK	6-12-79	
3	UPDATE ARTWORK	8-9-79	
4	REVISED PER ECN 2851	10-26-79	
5	REVISED PER ECN 2967	11-7-79	
6	REVISED PER ECN 2874	11-15-79	
7	REVISED PER ECN 2905	11-27-79	
8	REV PER ECN 2917	12-12-79	
9	REV PER ECN 3052	2-26-80	
10	REV PER ECN 3109	3-12-80	
A	PRODUCTION RELEASE	5-16-80	
B	REV. PER ECN # 3479	8-6-80	



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ENGINEER		8-9-79
PROJECT ENGINEER		
MFG ENGINEER		

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Appendix F -- MPI Diskette Drive Description

Crider
Stuml

SPECIFICATIONS

DOUBLE DENSITY SINGLE SIDED
40 TRACK DISKETTE DRIVE

PRELIMINARY
For Reference Only

DEC 17 1980

SYM	REVISIONS	DATE	APPROVED
1	PRELIMINARY RELEASE		

SHEET 1 OF 20 19

ATARI

DOUBLE DENSITY SINGLE SIDED
40 TRACK DISKETTE DRIVE

DRAWN BY	ENGINEERG. MGR.	MATERIAL
CHECKED	QUAL. ASSURANCE	DRAWING NO. C016890
ENGINEER	MFG ENGINEERG.	

1.0 SCOPE

THIS SPECIFICATION DEFINES THE GENERAL, PHYSICAL AND ELECTRICAL REQUIREMENTS FOR THE M51-1 MINI DISKETTE FLOPPY DISK DRIVE. THE M51-1 IS A SINGLE SIDED DOUBLE DENSITY 40 TRACK DRIVE.

2.0 GENERAL REQUIREMENTS

2.1 ENVIRONMENT

2.1.1 OPERATION AND STORAGE

THE M51-1 SHALL WITHSTAND OPERATION AND STORAGE TEMPERATURE IN THE RANGE OF 50°F TO 125°F (10°C TO 51.6°C) AT A RELATIVE HUMIDITY OF 8% TO 80%. THE WET BULB READING SHALL NOT EXCEED 85°F (29.4°C). THE DISK MUST BE ACCLIMATIZED IN THE OPERATING ENVIRONMENT FOR A MINIMUM OF ONE HOUR PRIOR TO USE. THERE SHALL BE NO MOISTURE ON OR IN THE DRIVE.

2.1.2 TEST

UNLESS OTHERWISE STATED, MEASUREMENTS SHALL BE CARRIED OUT AT AMBIENT CONDITIONS OF 74 ± 5°F (22.8 ± 2.8°C) AND 40% TO 60% RELATIVE HUMIDITY AFTER 24 HOURS OF ACCLIMATIZATION.

2.1.3 TRANSPORTATION

WHEN PACKED FOR SHIPMENT, TEMPERATURES OF -40°F TO 125°F (-40°C TO 51.6°C) ARE ALLOWABLE WITH RELATIVE HUMIDITY OF 8% TO 90%. NO MOISTURE SHALL CONDENSE ON, OR IN THE ASSEMBLY.

2.2 MEAN TIME BETWEEN FAILURES (MTBF)

THE MTBF OF THE 550 IS 9,000 HOURS. THE MTBF IS DEFINED:

$$\text{MTBF} = \frac{\text{OPERATING HOURS}}{\text{UNSCHEDULED INCIDENTS}}$$

UNSCHEDULED INCIDENTS ARE DEFINED AS FAILURES NECESSITATING REPAIR, ADJUSTMENT, OR REPLACEMENT ON AN UNSCHEDULED BASIS.

2.3 MEAN TIME TO REPAIR (MTTR)

THE MTTR SHALL NOT EXCEED 0.5 HOURS PER INCIDENT. MTTR IS DEFINED AS THE AVERAGE TIME FOR TRAINED SERVICE PERSONNEL TO DIAGNOSE AND REPAIR A FAILURE IN THE 550 FLEXIBLE DISK DRIVE.

2.4 REFERENCE DOCUMENTS

2.4.1 FLEXIBLE DISK DRIVE DWG CA014072

2.4.2 MODEL 810 DWG CA014162

2.4.3 FIELD SERVICE MANUAL 810 DISK DRIVE

3.0 IDENTIFICATION AND DATA

TEST RESULTS OF EACH UNIT TESTED SHALL BE MAINTAINED. THE TEST RESULT DATA SHEET SHALL IDENTIFY THE UNIT TESTED AS FOLLOWS:

3.1 PART NUMBER OF THE DISKETTE DRIVE PLUS PART NUMBERS OF THE INCLUDED OPTIONS.

3.2 SERIAL AND PART NUMBER AND REVISION LETTER OF THE DISKETTE DRIVE.

3.3 SERIAL AND PART NUMBER AND REVISION LETTER OF THE READ/WRITE HEAD.

3.4 SERIAL AND PART NUMBER AND REVISION LETTER OF THE CE DISKETTE USED FOR ALIGNMENTS.

4.0 TEST ASSEMBLY

4.1 UNLESS OTHERWISE STATED ALL TESTS SHALL BE CONDUCTED USING THE ATARI 810 ELECTRONICS.

5.0 MECHANICAL REQUIREMENTS

5.1 OVERALL MECHANICS

5.1.1 WEIGHT

INSURE THAT THE UNIT DOES NOT WEIGH MORE THAN 4.0 LBS.

5.1.2 DIMENSIONS

SEE DWG # CA014072.

SYM	REVISIONS	DATE	APPROVED
	SEE SHEET 1		

ATARI

DOUBLE DENSITY SINGLE SIDED
40 TRACK DISKETTE DRIVE

DRAWN BY	ENGINEERG. MGR.	MATERIAL
CHECKED	QUAL. ASSURANCE	DRAWING NO.
ENGINEER	MFG. ENGINEERG.	C016890

5.2 HEAD/CARRIAGE ASSEMBLY

5.2.1 HEAD POSITION

INSURE THAT THE HEAD IS PROPERLY ALIGNED IN THE CARRIAGE.

GAP LOCATION - .625 $\pm$.002 REF SHAFT CENTERLINE

GAP AZIMUTHAL MISALIGNMENT - 0° $\pm 0^{\circ}$ 12'

CROWN LOCATION - .230 $\pm$ .0025 REF SHAFT CENTERLINE

5.2.2 HEAD LOAD PAD FORCE

INSURE THAT THE PAD FORCE IS 17.0 $\pm$ 2.0 GRAMS

5.2.3 HEAD/HUB/BOSS HEIGHTS

HEAD	.000
HUB	-.010/-.015
BOSS	-.015/-.050

5.2.4 SPINDLE FACE RUNOUT

WITHIN .001

5.2.5 UPPER ARM CENTERING

WITHIN .010

5.2.6 HEAD CABLE ROUTING

ALONG LEFT HAND GUIDE

5.3 DRIVE BELT/SPINDLE SYSTEM

5.3.1 INSURE THAT THE BELT TENSION IS 15 $\pm$ 1 oz/LEG ON INSTALLATION OF NEW BELT.

5.3.2 INSURE THAT THE BELT TRACKS IN THE CENTER OF BOTH PULLEYS.

5.3.3 INSURE THAT THE STROBE LABEL ON THE SPINDLE PULLEY HAS A MAXIMUM ECCENTRICITY OF 0.010 INCH.

5.3.4 INSURE THAT THE SPINDLE TORQUE, WITH THE DOOR OPEN AND NO DRIVE BELT INSTALLED, DOES NOT EXCEED 0.5 OZ-IN.

5.3.5 INSURE THAT THE SPINDLE I.D. RUNOUT DOES NOT EXCEED .0009 INCH TIR.

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5.3.6 INSURE THAT THE SPINDLE FACE RUNOUT DOES NOT EXCEED 0.001 INCH TIR.

5.3.7 INSURE THAT THE SPINDLE FACE IS PARALLEL TO PLANE -A- WITHIN 0.0015 INCH.

5.4 OVERALL DRIVE PARAMETERS

5.4.1 INSURE THAT THE DISKETTE GUIDE SPAN IS 5.280 ±.005 INCHES.

5.4.2 INSURE THAT THE DISKETTE GUIDES ARE SYMMETRICAL ABOUT THE HUB CENTERLINE WITHIN 0.010 INCH TOTAL.

5.4.3 INSURE THE THE FRONT DOOR IS CENTERED WITHIN THE OPENING IN THE FRONT PLATE WITHIN .020 INCH.

5.4.4 INSURE HEAD IS PARALLEL TO SURFACE -A- WITHIN .002 TIR.

5.4.5 INSURE THAT THE SPINDLE FACE IS .010 TO .015 INCH BELOW HEAD.

5.4.6 INSURE THAT DISKETTE LOAD BOSS IS .035 TO .050 INCH BELOW HEAD.

5.4.7 INSURE THAT THE SNAP RING ON THE CLUTCH PIN CLEARS THE CARRIER FRAME BY A MINIMUM .010 INCH WHEN THE DOOR IS CLOSED.

5.4.8 INSURE THAT THE CLUTCH CLEARS THE HUB FACE BY AT LEAST .070 INCH WHEN THE DOOR IS OPEN.

5.4.9 INSURE THAT THE EJECTOR MECHANISM DOES NOT BIND WHEN INSERTING A DISK. WHEN THE DOOR IS OPENED THE EJECTOR MUST PUSH THE DISKETTE OUT OF THE DRIVE BY ½ TO 1½".

6.0 ALIGNMENTS AND ADJUSTMENTS

6.1 TRACK POSITION

WITH STEPPER MOTOR PHASE 1 AND 4 ACTIVE, THE CARRIAGE POSITION SHALL BE ADJUSTED SUCH THAT THE READ/WRITE HEAD IS LOCATED OVER THE CENTER OF THE TRACK 16 ± .001 INCH.

6.2 TRACK 00 STOP

SET THE TRACK 00 STOP (ON CHASSIS) TO .010 ± .003 OUTSIDE OF THE TRUE TRACK 00 POSITION.

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6.3 SPINDLE DRIVE SYSTEM

6.3.1 ADJUST THE SPINDLE DRIVE MOTOR SPEED TO PRODUCE A SPINDLE SPEED OF 300 $\pm$ 1.5 RPM.

6.3.2 VERIFY THAT THE SPINDLE START TIME IS 0.5 SECOND MAXIMUM FROM 0 TO 300 RMP.

6.3.3 VERIFY THAT THE SPINDLE LATENCY IS 200 $\pm$ 1 MILLISECONDS.

6.3.4 FLUTTER $\leq$ 1.5% . THE INSTANTANEOUS SPEED VARIATION WITHIN ONE REVOLUTION.

6.3.5 WOW $\leq$ 1%. THE LONG TERM SPEED VARIATION.

6.4 HEAD ALIGNMENT

6.4.1 AZIMUTH: $0^{o} \pm 12'$

ANGULAR DISPLACEMENT OF READ/WRITE GAP FROM SHAFT CENTERLINE. THIS IS MEASURED BY USING A C.E. DISKETTE.

6.4.2 TRACK ALIGNMENT: $\geq$ 80%

ADJUSTMENT OF THE READ/WRITE CARRIAGE SUCH THAT IT IS IN RADIAL ALIGNMENT AS MEASURED BY THE PATTERN ON TRACK 16 OF THE C.E. ALIGNMENT DISKETTE.

6.4.3 HYSTERESIS: $\geq$ 80%

THE ERROR IN POSITIONING WHILE MOVING IN TO TRACK 16 VERSUS MOVING OUT TO TRACK 16.

6.5 HEAD PERFORMANCE

6.5.1 READ HEAD OUTPUT

THE READ HEAD APLITUDE FROM TRACK 00 TO 39 INCLUSIVE SHALL BE 2.30 mv MINIMUM AT 2F (125KHz).

RESOLUTION: $\geq$ 45%

"2F" AMPLITUDE DIVIDED "1F" AMPLITUDE MULTIPLIED BY 100% (BOTH AMPLITUDES AT THE SAME TRACK).

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6.5.2 AMPLITUDE VARIANCE

READ DATA AT TRACK 40 AS OBSERVED AT THE AMPLIFIED OUTPUT OF THE HEAD SHALL HAVE LESS THAN 10% TOTAL AMPLITUDE VARIANCE DUE TO RUNOUT AND COMPLIANCE.

6.5.3 ASYMMETRY $\leq$ 400 n sec.

NON-SYMMETRICAL OUTPUT OF THE READ CIRCUIT INDICATED BY A DIFFERENCE IN TIME PERIODS FROM ODD DATA PULSE TO EVEN DATA PULSE AND EVEN DATA PULSE TO ODD DATA PULSE.

6.5.4 RUNOUT $\leq$ 15% AMPLITUDE VARIANCE

MEAUSRE OF HOW WELL THE CLUTCH ASSEMBLY SEATS THE DISKETTE AGAINST THE SPINDLE HUB. THIS IS MEASURED BY WRITING A "1F" PATTERN AT TRACK 0-0 AND OBSERVING THE WORST CASE AMPLITUDE VARIANCE OBTAINED BY OPENING AND CLOSING THE DRIVE DOOR (ALLOWING THE CLUTCH ASSEMBLY TO RESEAT THE DISKETTE) TEN TIMES.

6.5.5 MAGNETIZATION $\leq$ 15% AMPLITUDE DECREASE

A MEASURE OF THE STRAY OR RESIDUAL MAGNETIC FIELDS WHICH ARE PRESENT IN THE READ/WRITE HEAD. THIS IS MEASURED BY WRITING A "1F" PATTERN ON TRACKS 16 AND 17, AND THEN STEPPING BACK AND FORTH ACROSS THE TWO TRACKS FOR 25 SECONDS. THE PERCENTAGE DECREASE IN AMPLITUDE AT EITHER TRACK IS A MEASURE OF MAGNETIZATION.

6.5.6 WRITE CURRENT

THE WRITE CURRENT SHALL BE 8.5 $\pm$ 0.6 MILLIAMPS PEAK-TO-PEAK WITH NOMINAL POWER SUPPLY VOLTAGE.

6.5.7 ERASE CURRENT

THE ERASE CURRENT SHALL BE 80 $\pm$ 12 MILLIAMPS.

6.5.8 ERASE SWEEP

EACH ERASE POLE SHALL ERASE PREVIOUSLY WRITTEN DATA TO A RESIDUAL SIGNAL OF EQUAL TO OR LESS THAN 15% OF THE ORIGINAL DATA WITH I_E EQUAL TO OR GREATER THAN 68 MA.

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6.5.8 (CONTINUED)

MEASURE OF HOW MUCH OF A REDUCTION IN AMPLITUDE IS OBTAINED WHEN NOMINAL ERASE CURRENT FLOWS THROUGH THE ERASE COIL OF THE READ/WRITE HEAD. THIS IS MEASURED BY WRITING A "1F" PATTERN AT TRACKS 16 OF 17, AND THEN SEEKING BACK AND FORTH BETWEEN THE TWO TRACKS FOR 15 SECONDS, WITH ERASE CURRENT ON. THE PERCENTAGE DECREASE FROM THE ORIGINAL AMPLITUDE IS A MEASURE OF ERASE EFFICIENCY.

6.5.9 COMPLIANCE 10% AMP DECREASE

MEASURE OF HOW WELL THE DISKETTE IS "WRAPPED AROUND" THE CROWN OF THE READ/WRITE HEAD. THIS IS MEAUSRED BY WRITING A "1F" PATTERN AT THE INNERMOST TRACK WHILE PLACING A 12±2 GRAM WEIGHT ABOVE THE PRESSURE PAD ON THE UPPER ARM. THE AMPLITUDE OBTAINED IS OBSERVED, THEN THE PRESSURE IS REMOVED FROM THE UPPER ARM AND THE NEW AMPLITUDE IS OBSERVED. THE DECREASE IN AMPLITUDE IS A MEASURE OF COMPLIANCE.

6.6 STEPPER PERFORMANCE

6.6.1 STEP TIME

THE CARRIAGE SHALL BE CAPABLE OF REPEATED STEPS IN EITHER DIRECTION WHEN STEP SIGNALS OCCURRING AT 5.0 ms INTERVALS ARE APPLIED.

6.6.2 STEP SETTLE TIME

READ DATA AS OBSERVED AT THE AMPLIFIED OUTPUT OF THE HEAD SHALL BE $\geq$90% STABLE IN AMPLITUDE WITHIN A 20 ms PERIOD AS MEASURED FROM THE TRAILING EDGE OF THE STEP SIGNAL FOR ALL OPERATING ORIENTATIONS OF THE DISKETTE DRIVE.

7.0 WRITE PROTECT

THE WRITE PROTECT IS TESTED BY INSERTING A NON WRITE PROTECTED DISKETTE AND VERIFYING A106 PIN 14 IS $\leq$ 0.4U. THEN INSERT A WRITE PROTECTED DISK AND VERIFY A106 PIN 14 IS $\geq$ 4V.

8.0 READ/WRITE HEAD - GENERAL SPECIFICATIONS

THE HEAD SHALL BE MECHANICALLY AND FUNCTIONALLY SIMILAR TO THE IBM FD-33 DISKETTE DRIVE HEAD.

8.1 PHYSICAL REQUIREMENTS

8.1.1 HEAD TYPE

SINGLE R/W GAP WITH SEPARATE TUNNEL ERASE.

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8.1.2 HEAD/MEDIA INTERFACE

IN CONTACT, CERAMIC AND FERRITE WEAR SURFACES.

8.1.3 READ/WRITE GAP

100 MICROINCHES, REFERENCE

8.1.4 CROWNED FACE SURFACE QUALITY

SURFACE FINISH - CROWNED CERAMIC/FERRITE FACE SHALL BE 3 MICROINCHES AA OR BETTER.

GAP ZONE - CORE FACE AREAS WITHIN +.005" OF R/W AND ERASE GAPS SHALL HAVE GAP DEFECTS .0005" TOTAL LENGTH AND .0005" WIDE IN EACH AREA AND SHALL HAVE EDGE CHIPS .0003" IN TRACK WIDTH DIRECTION AND .0005" LONG. NO MORE THAN (2) DISCONTINUITIES PER HEAD SHALL BE ALLOWED.

NON-GAP ZONE - OTHER FACE AREAS SHALL HAVE NO CHIPS ON CORES, SPACERS OR CORE EDGES LARGER THAN .002". NO MORE THAN (5) CHIPS PER HEAD ARE ALLOWED.

SCRATCHES - SCRATCHES SHALL BE .0002" MAX WIDTH BY .000050" MAX DEEP. THE TOTAL SCRATCH LENGTH PER HEAD SHALL NOT EXCEED .015".

8.1.5 CLEANING

THE HEAD CONTRUCTION SHALL ALLOW PERIODIC CLEANING WITH METHYL-ALCOHOL OR 1-1-1 TRICHLORETHANE WITHOUT HARM.

8.2 PERFORMANCE REQUIREMENTS

8.2.1 TEMPERATURE RANGE

0 TO +50°C, OPERATING; -45 TO +71°C STORAGE.

8.2.2 HUMIDITY RANGE

8 TO 80% Rh, OPERATING; 8 TO 90%, NONCONDENSING, STORAGE.

8.2.3 DESIGN LIFE

16,000 HOURS IN CONTACT WITH DISKETTE AT 17 GRAMS PRESSURE PAD FORCE.

8.2.4 PRESSURE PAD FORCE

17 ± 2 GRAMS OVER A .156" DIAMETER PAD.

8.2.5 RECORDING METHOD

DOUBLE FREQUENCY, MFM, M^2FM, GCR

8.2.6 RECORDING MEDIA

FLEXIBLE DISK PER ATARI SPECIFICATION C016884

8.2.7 HEAD/MEDIA VOLOCITY

45 TO 70.7 INCHES/SEC. AT 300 RPM

8.2.8 DISK SPEED

300 $\pm$3 RPM.

8.2.9 DATA PACKING DENSITY

UP TO 2760 BITS/INCH (5520 FCI) AT 300 RPM.

8.2.10 WRITE CURRENT *

8.5MA $\pm$5% PEAK-PEAK

8.2.11 ERASE CURRENT *

80 $\pm$8MA

8.2.12 READ OUTPUT *

GREATER THAN 3.0MV PEAK-PEAK AT 5520 FCI (45IPS)
LESS THAN 10.0MV PEAK-PEAK AT 1768 FCI (70.7 IPS)

8.2.13 RESOLUTION

$$\frac{\text{E OUT @ 5520 FCI}}{\text{E OUT @ 2760 FCI}} \geq 0.55 \text{ (45 IPS)}$$

$$\frac{\text{E OUT @ 3536 FCI}}{\text{E OUT @ 1768 FCI}} \leq 0.95 \text{ (70 IPS)}$$

8.2.14 OUTPUT WAVEFORM ASYMMETRY*

PERIOD FROM POSITIVE TO NEGATIVE PEAK, PERIOD FROM NEGATIVE TO POSITIVE PEAK, (LONGER PERIOD) - SHORTER PERIOD) $\leq$ 400ns

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8.2.15 ERASE SWEEP*

RESIDUAL OUTPUT AFTER TRAVERSING A WRITTEN TRACK WITH ONLY THE ERASE COIL ENERGIZED $\frac{(\text{E OUT AFTER SWEEP})}{\text{E OUT BEFORE SWEEP})} \leqq 0.05$ EACH POLE

8.2.16 READ OUTPUT REDUCTION DUE TO TUNNEL ERASE

$\frac{(\text{E OUT W/TUNNEL ERASE})}{(\text{E OUT WITHOUT TUNNEL ERASE})} \geqq 0.9$

8.2.17 SELF ERASURE

THE OUTPUT SIGNAL LEVEL SHALL BE DECREASED BY NO MORE THAN 5% FROM ITS INITIAL VALUE AFTER (10) SWEEPS ACROSS THE RECORDED TRACK BY THE NON-ENERGIZED HEAD.

8.2.18 ERASE/WRITE DELAY

WRITE WINDING ON, THEN ERASE ON 430ns ±20%

WRITE WINDING OFF, THEN ERASE OFF 850ns ±20%

8.2.19 POLARITY

IF THE VOLTAGE AT CONNECTOR PIN 6 IS MADE POSITIVE WITH RESPECT TO PIN 5, CURRENT WILL FLOW IN THE ERASE WINDING SUCH THAT THE TRAILING POLE OF THE ERASE GAP IS A NORTH POLE.

IF THE VOLTAGE AT CONNECTOR PIN 3 IS MADE POSITIVE WITH RESPECT TO PIN 1, CURRENT WILL FLOW IN THE READ/WRITE WINDING SUCH THAT THE TRAILING POLE OF THE READ/WRITE GAP IS A NORTH POLE.

8.2.20 OVERWRITE MODULATION*

THERE SHALL BE NO MORE THAN 10% MODULATION OF A ONE-REVOLUTION WRITE AT 125 KHz ON A TRACK PREVIOUSLY WRITTEN AT 67.5 KHz FOR AT LEAST (10) REVOLUTIONS.

8.3 ELECTRICAL PARAMETERS

8.3.1 INDUCTANCE*

READ/WRITE, PER LEG = 325 ±65 µH
BALANCE, LEG TO LEG = 0.95
ERASE ≦ 30 µH @ 1 kHz

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8.3.2 RESISTANCE*

READ/WRITE, PER LEG = 10.0 OHMS, MAX.
ERASE = 4.0 OHMS, MAX.

8.3.3 RESONANCE FREQUENCY*

GREATER THAN 450 kHz.

8.3.4 INSULATION RESISTANCE

GREATER THAN 50M OHMS @ 200 Vdc BETWEEN COILS AND CORE.

8.3.5 GROUNDING

BACK BAR OF R/W CORE SHALL BE ELECTRICALLY BONDED TO R/W COIL CENTER TAP.

8.4 TEST CONDITIONS

8.4.1 TEST AMPLIFIER

THE AMPLIFIER WHICH WILL BE USED TO TEST READ/WRITE PARAMETERS SHALL HAVE AN INPUT IMPEDANCE OF 4.70K OHMS SHUNTED BY 10 pF.

8.4.2 QUALIFIED VENDOR PERFORMANCE

TO ACHIEVE QUALIFIED VENDOR STATUS, THE MANUFACTURER MUST CONSISTENTLY SUPPLY 95% ACCEPTABLE PARTS PER THIS SPECIFICATION.

* MEASURED AT CONNECTOR TERMINALS ON END OF 12.00" LONG CABLE

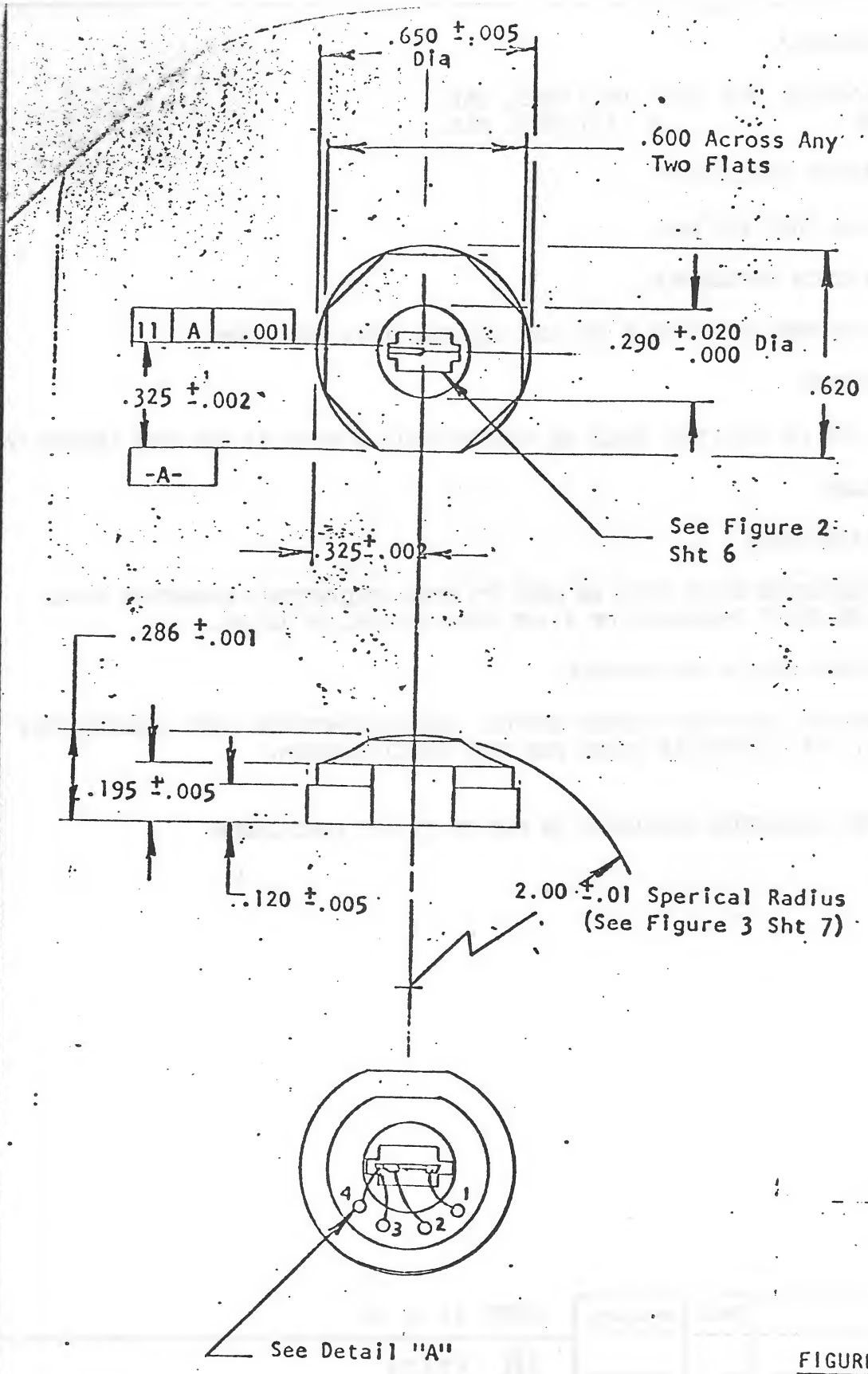
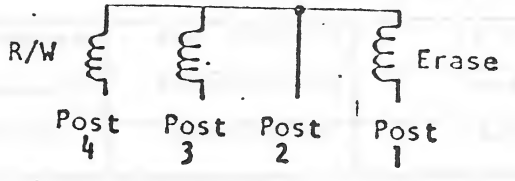


FIGURE 1



Detail -A-

CO 16890

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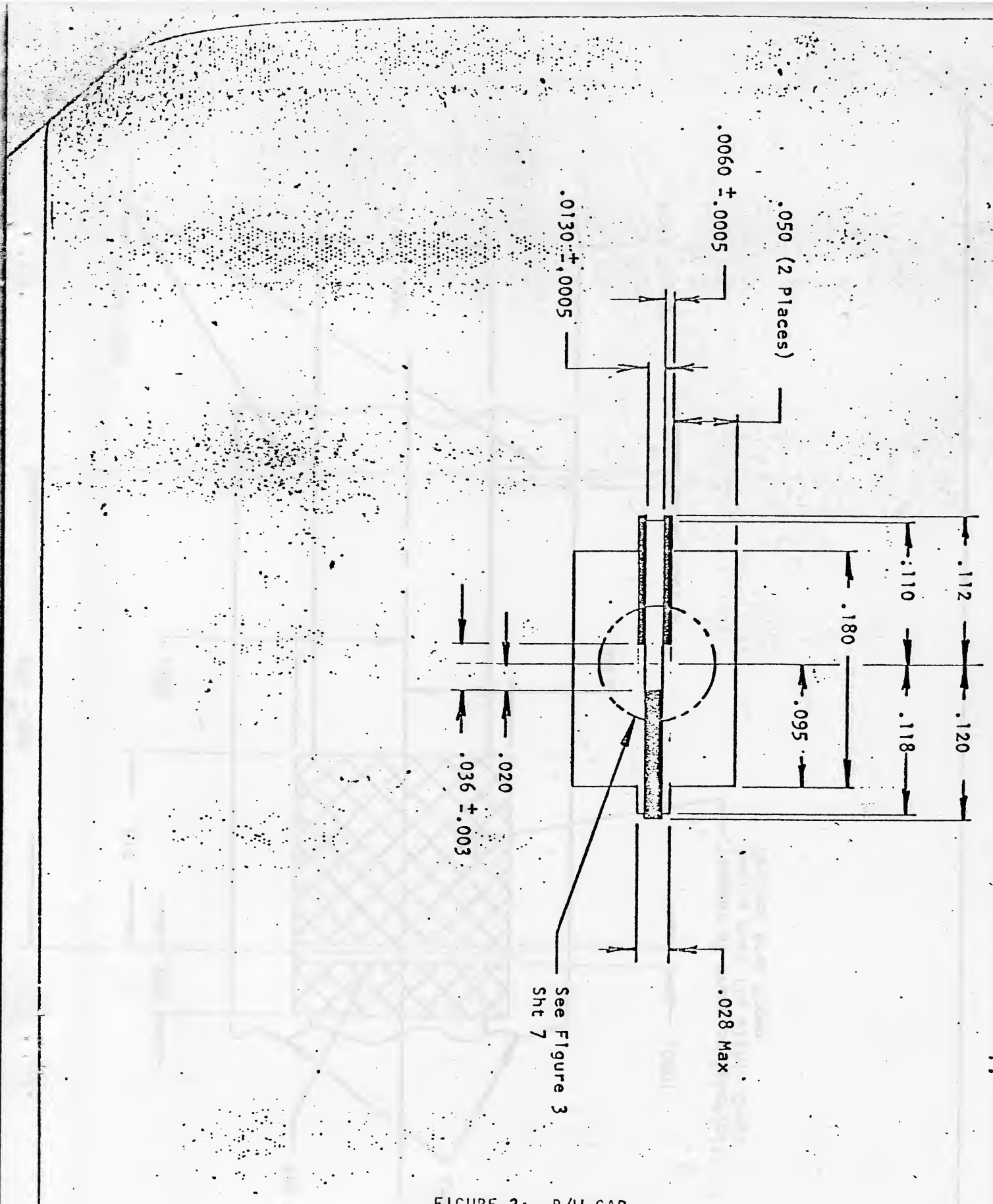

FIGURE 2: R/W GAP

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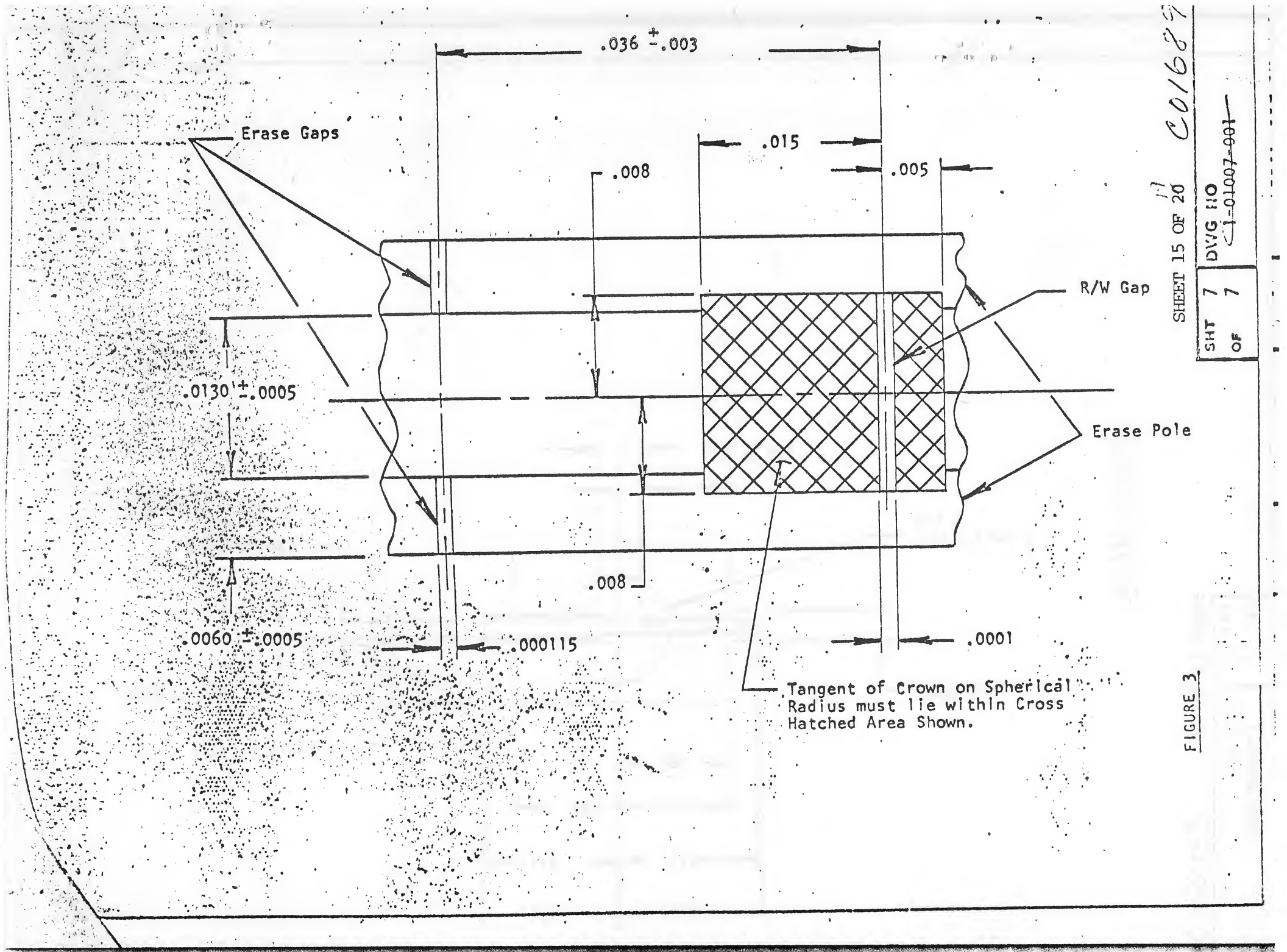
SHT 6 OF 7	DWG NO 1-01007-001	R E



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C01682

FIGURE 3

9.0 DRIVE, MOTOR

9.1 SOURCE: (a) BUEHLER PRODUCTS, INC.
P/N 13.65.28

9.2 CHARACTERISTICS

9.2.1	CURRENT:	300 mA
9.2.2	VOLTAGE:	8 VDC ± 15%
9.2.3	TORQUE: LOAD	MIN 1.0 IN. OZ. @ 2500 RPM & 8V
9.2.4	SPEED:	NOMINAL 2500 RPM
9.2.5	TERMINAL RESISTANCE:	9.2 ± 10%
9.2.6	TORQUE CONSTANT:	2.25 OZ. IN./A ± 10%
9.2.7	VOLTAGE CONSTANT:	1.6 V/K RPM ± 10%
9.2.8	TYPICAL MOTOR LIFE:	1500 HRS. WITH 2 LBS SIDE LOAD @ 2500 RPM

9.3 TACHOMETER GENERATOR:

9.3.1	OUTPUT:	1.85 VRMS ± .2V/1000 RPM INTO 10KΩ LOAD.
9.3.2	LINEAR:	WITHIN 0.5% OVER ± 10% SPEED DEVIATION FROM 2500 RPM
9.3.3	DISTORTION:	WITHIN 8% AT 400 CYCLES.
9.3.4	CYCLE RATE TACH./ MOTOR	8/1

9.4 ROTATION: CCW LOOKING AT SHAFT END.

9.5 ENVIRONMENTAL REQUIREMENTS

9.5.1 TEMPERATURE RANGE

OPERATING:	50° TO 105°F
STORAGE/TRANSIT:	-30° TO 150°F

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ENGINEER	MFG ENGINEERG.	

9.5.2 RELATIVE HUMIDITY

OPERATING: 20% TO 80%

STORAGE/TRANSIT: 5% TO 95%

9.5.3 ALTITUDE

OPERATING: 1000 FEET BELOW TO 10,000 FEET ABOVE SEA LEVEL.

STORAGE/TRANSIT: SEA LEVEL TO 45,000 FEET ABOVE SEA LEVEL.

9.5.4 MAXIMUM WET BULB TEMPERATURE (ALL CONDITIONS)

$80^{O}F$

9.6 A 1000 PF $^{+80}_{-20}$% CAPACITOR IS TO BE MOUNTED INTERNALLY FROM EACH COMMUTATOR BRUSH TO CASE GROUND FOR MINIMIZING EMI.

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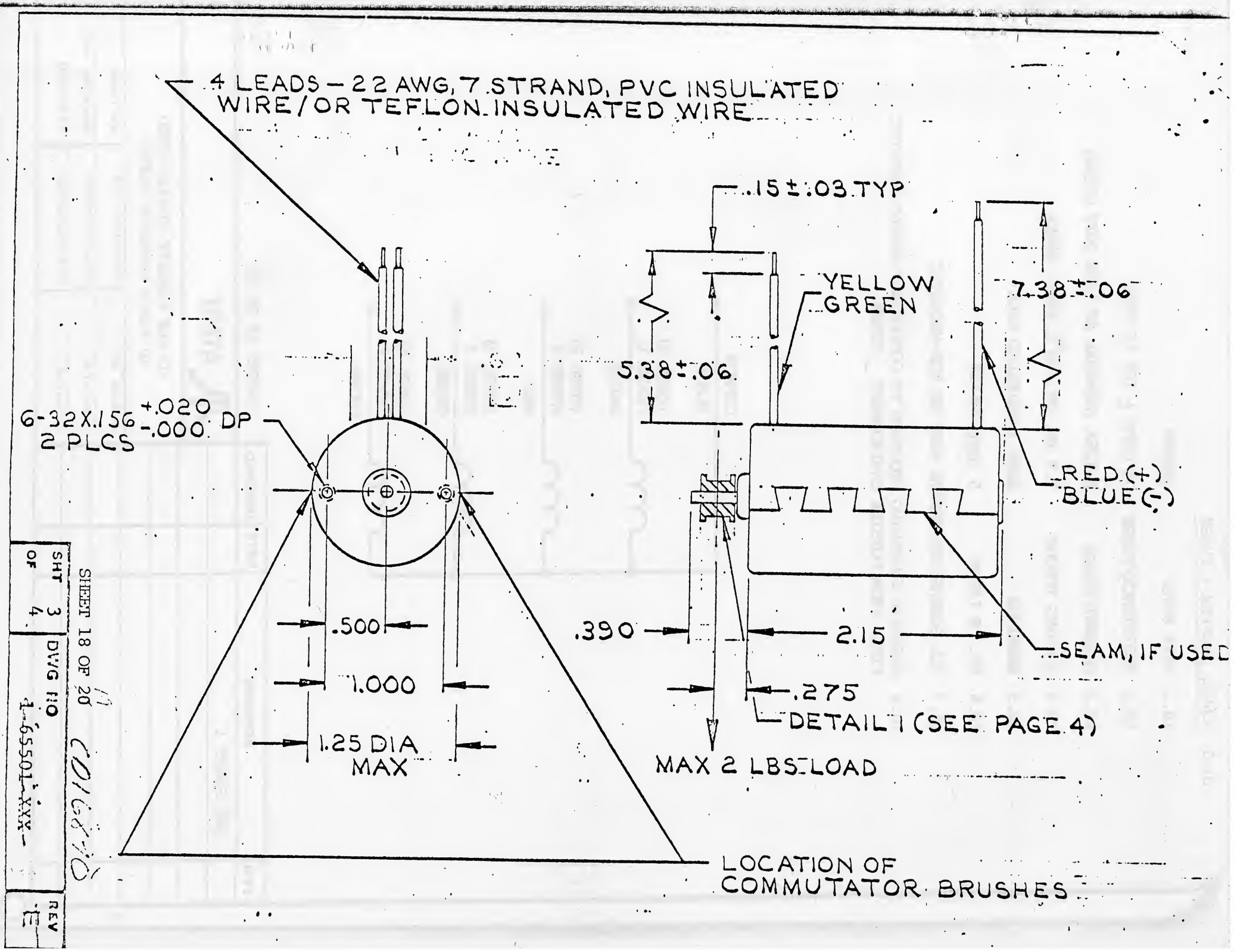

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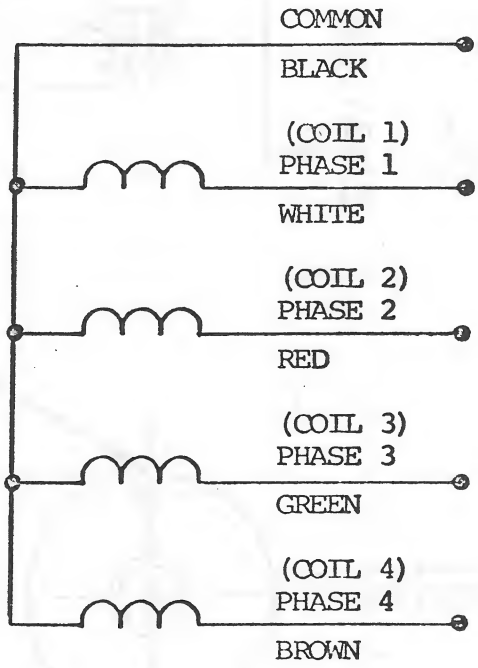
CD1668-10

10.0 MOTOR, STEPPER 4 PHASE

10.1	STEP RATE	200PPS
10.2	RESISTANCE/PHASE	75 OHMS ± 10% DC RES.
10.3	CURRENT/PHASE	0.125A (NOMINAL AT 100% DUTY CYCLE)
10.4	HOLDING TORQUE	7.8 IN. OZ. (35°C TEMP. RISE)
10.5	BEARINGS	ABEC 1 SHIELDED BALL
10.6	NO. OF LEADS	5 (UNI-POLAR)

10.7 ALL SCREWS AND SHAFTS MUST BE NON-MAGNETIC

10.8 MAGNETIC SHIELDING REQUIRED TO COMPLETELY SHEILD MAGNETIC FIELD FROM OUTSIDE ENVIRONMENT _ GUASS.



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